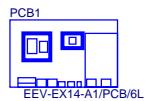


BLOCK DIAGRAM

Page	Function
01	BLOCK DIAGRAM
02	COM EXPRESS CONNECTOR
03	USB2.0(0-5) 、USB3.0(0-3)
04	AUDIO(ALC892)
05	VGA 、LVDS
06	PCIE SWITCH
07	LAN1 、LAN2(RTL8111E)
08	MINI PCIE CARD 、EXPRESS CARD
09	PCIEX1 、PCIEX4 、CLOCK BUFFER
10	PCIEX16
11	HDMI 、DISPLAY
12	DDI SLOT
13	SATA 、SD 、DIO
14	SUPER I/O(NCT6776F)
15	COM1 、COM2
16	KB 、MS 、PRT 、FDC 、BAT 、FAN
17	V5A 、ErP 、FRONT
18	V3.3A 、V5S 、V3.3S(TPS51220)
19	ATX & AT POWER(LTC3780:12V)
20	BIOS(SPI 、FWH)
21	LVDS&eDP
22	POWER DISTRIBUTION
23	MODIFY HISTORY

PCB p/n : E1907EX1404RO A11

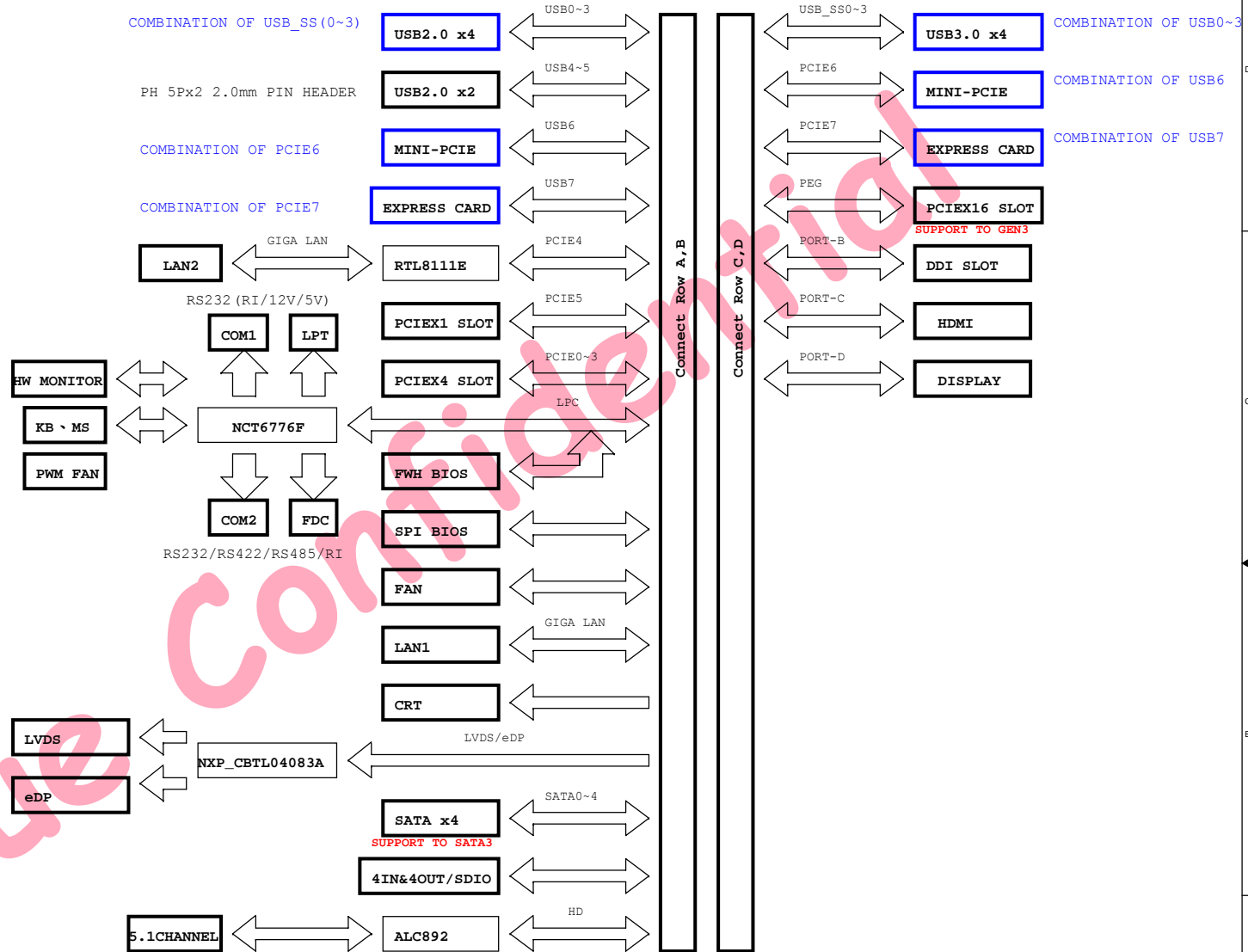


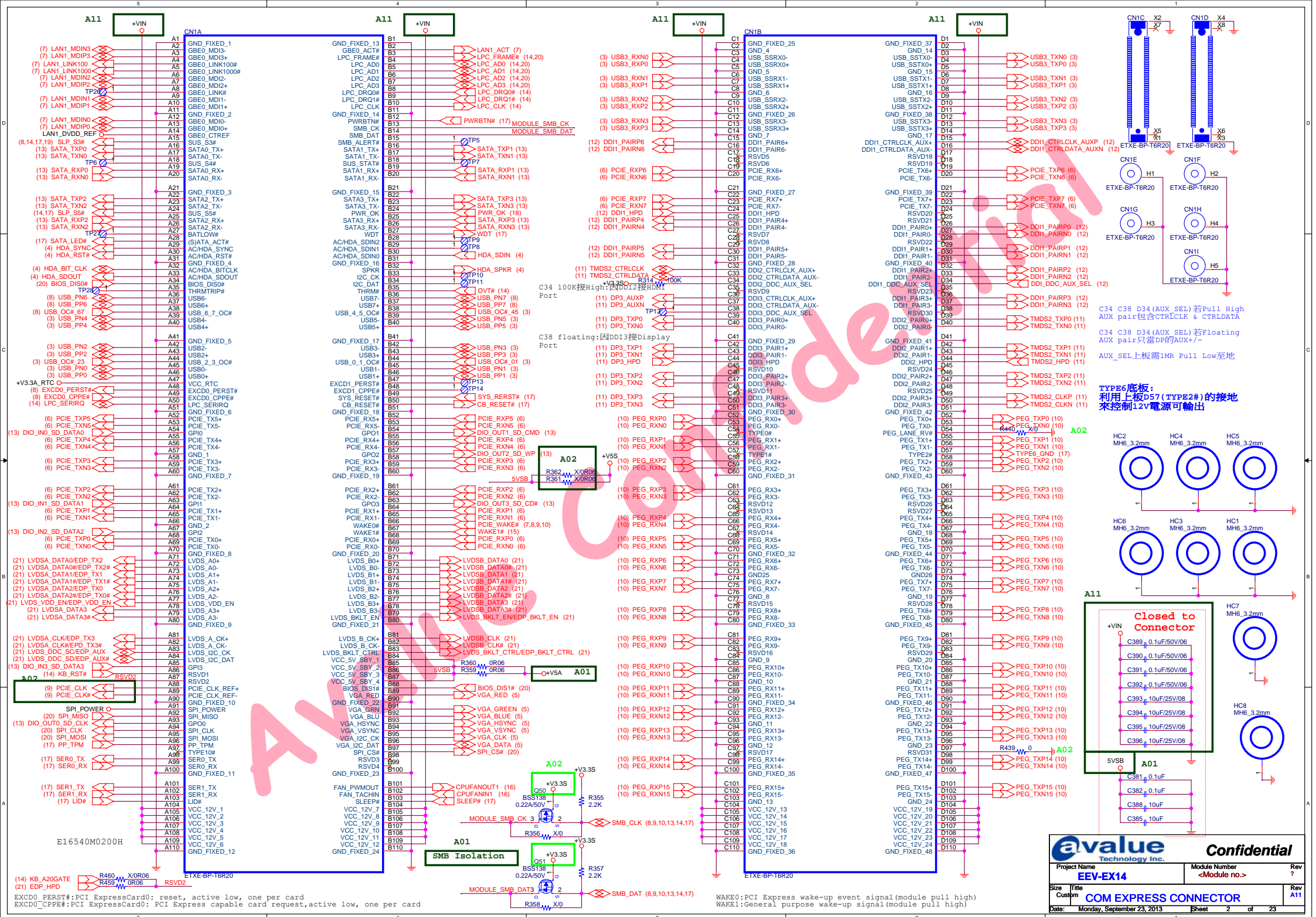
文字標示:
EEV-EX14 A11
E1907EX1404RO
MADE IN TAIWAN

LAYOUT NOTE:紅色字 或 紅色框 或 CLOSE TO... 或 LAYOUT...

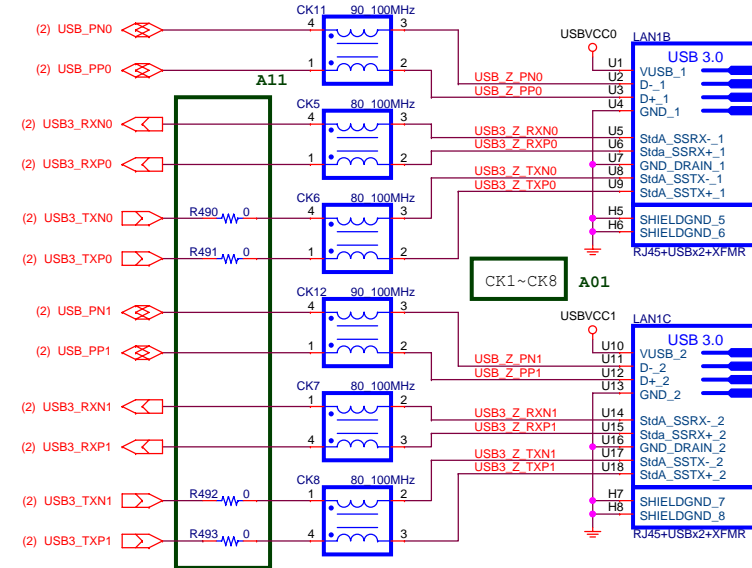
電阻部份
1. 0402不標示
2. 5%不標示
3. 1%及非0402要做標示
如10KR06/1%

電容部份
1. 0402不標示,但10uF全為0805也不標
2. 10uF(0805)及0.1uF(0402)的16V也不標
3. 0.1uF少數耐壓50V的,均用0603,均需做標示
4. 電容均用X5R X7R 除耐大電壓之電容
5. 其他uF pF電壓值不標示,因均大於16V

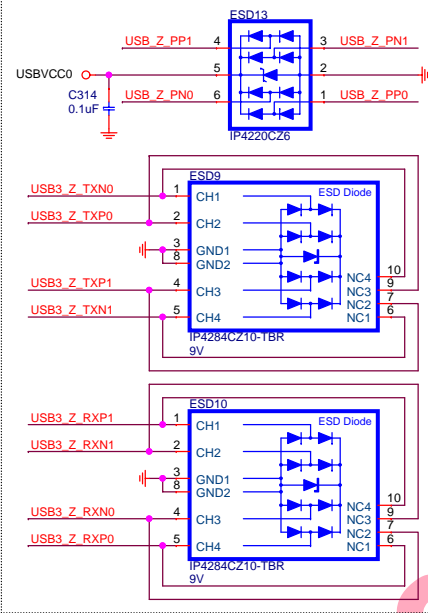




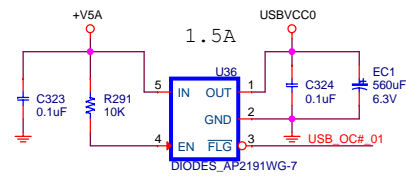
USB0 and USB1(USB2.0+USB3.0)



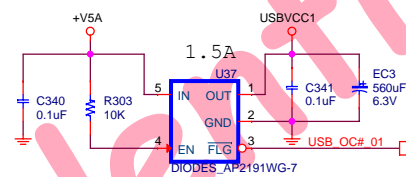
Closed to Connector



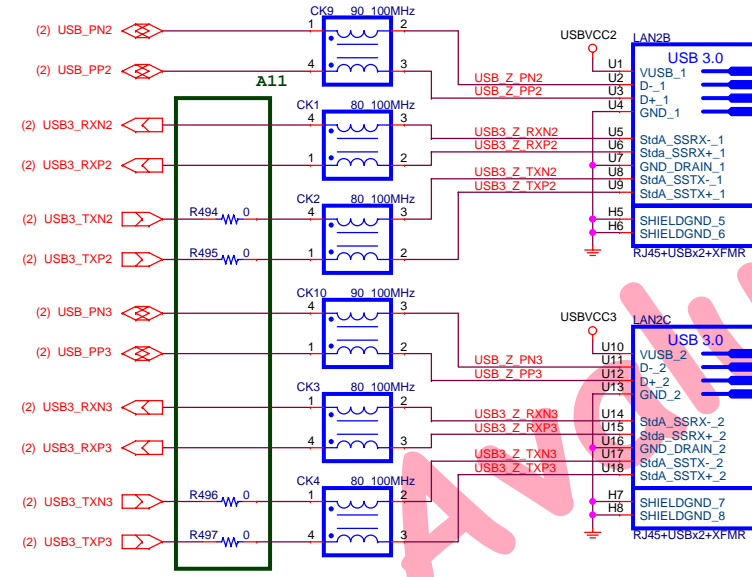
OC Pull High於上板



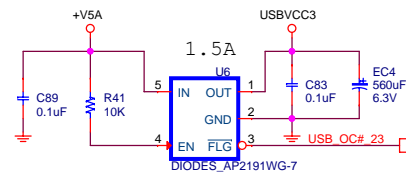
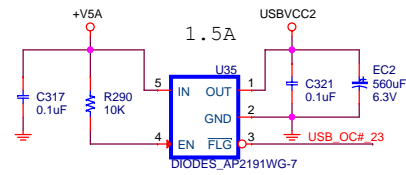
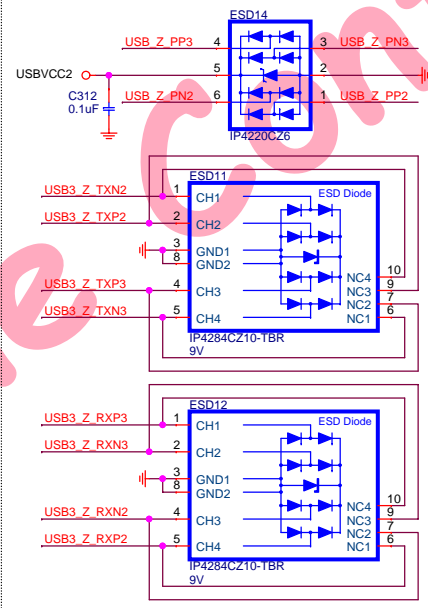
USB 2.0-->480Mbps (bit width 2083ps)
 USB 3.0-->5Gbps (bit width 200ps)
 USB 2.0-->5x100mA=0.5A
 USB 3.0-->6x150mA=0.9A
 公板 1 USB port 放220uF
 USB0~USB3 MAX 1.5A/Port



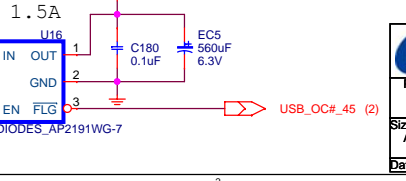
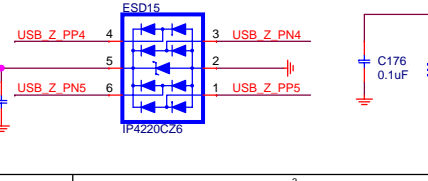
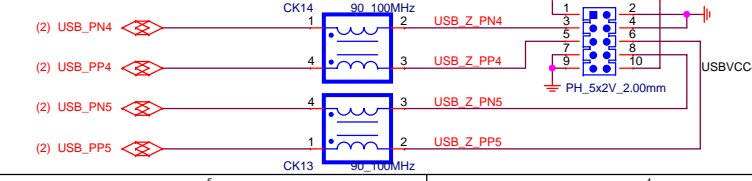
USB2 and USB3(USB2.0+USB3.0)



Closed to Connector



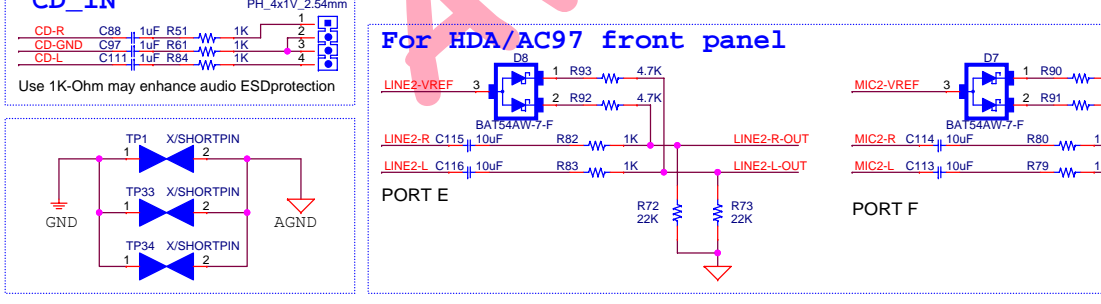
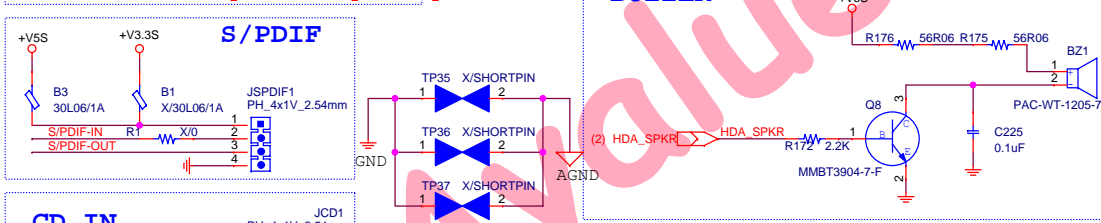
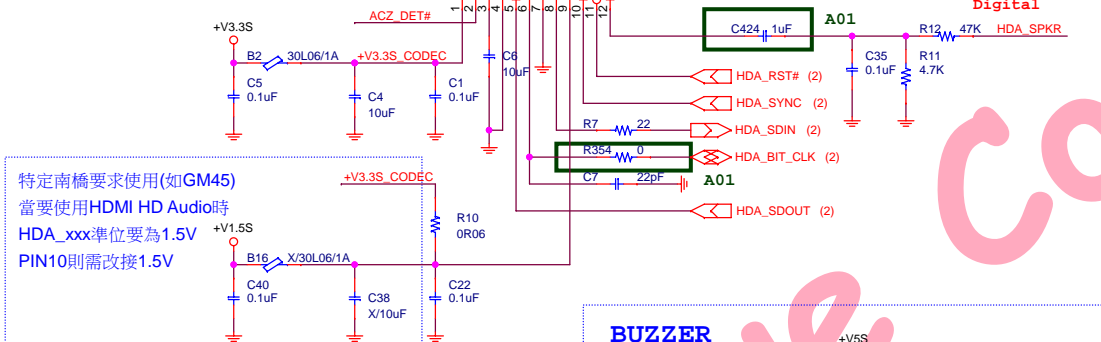
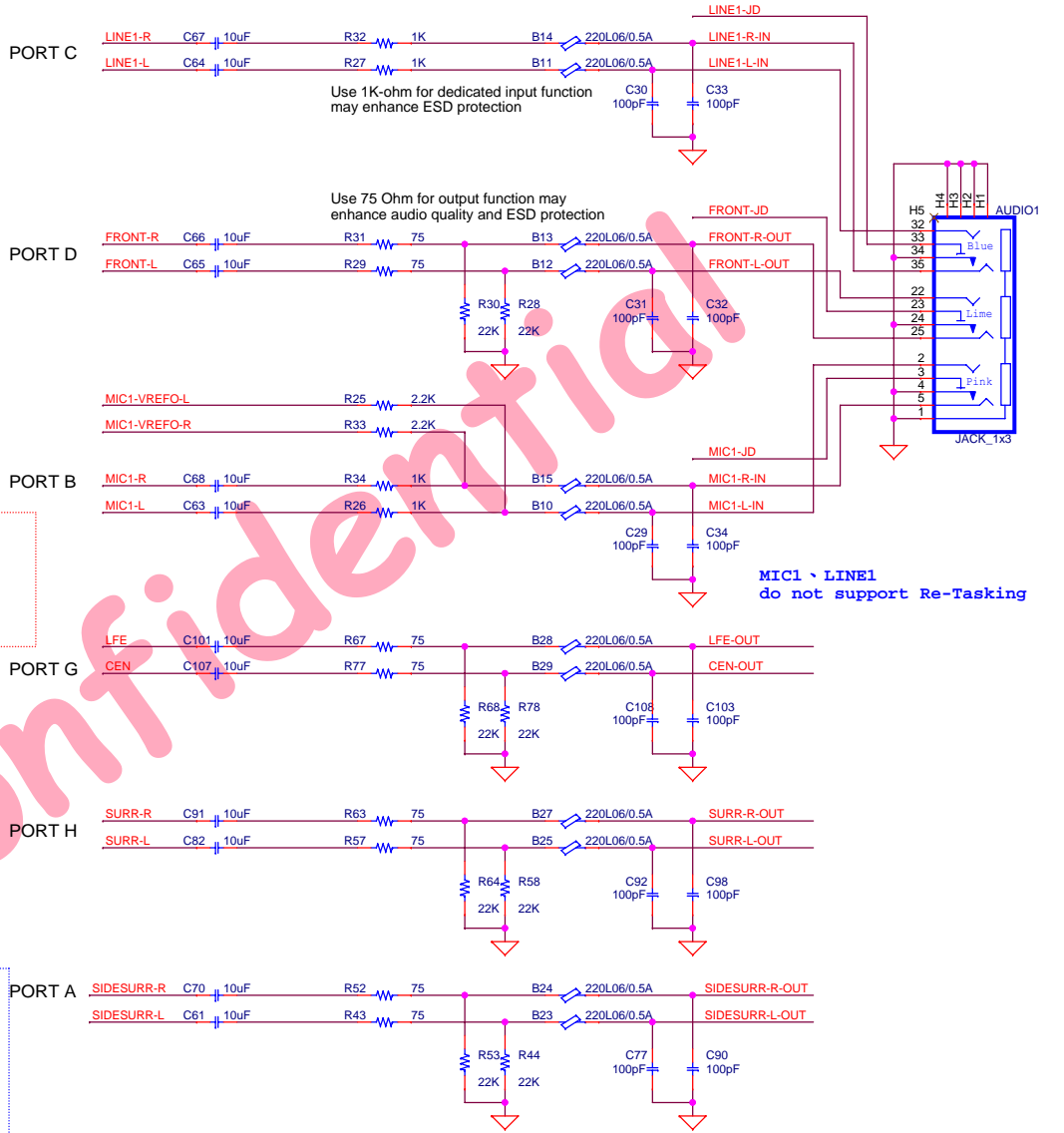
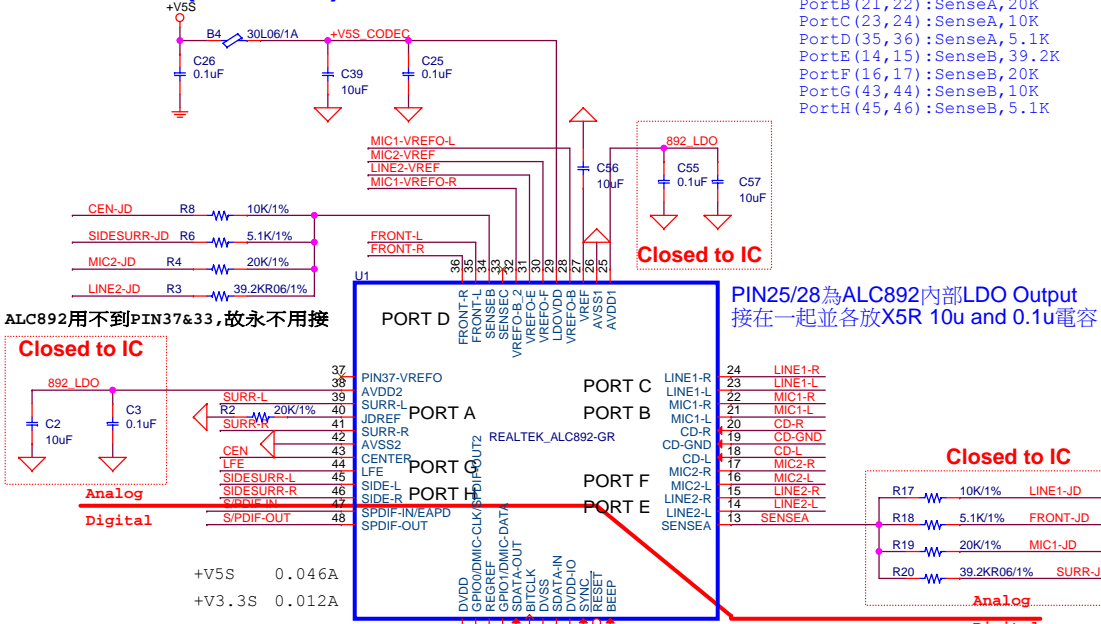
USB4 and USB5(USB2.0)



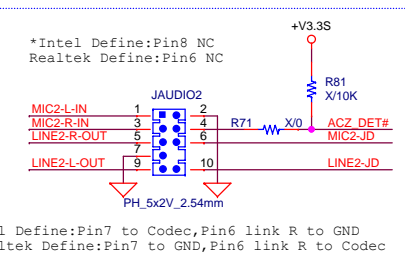
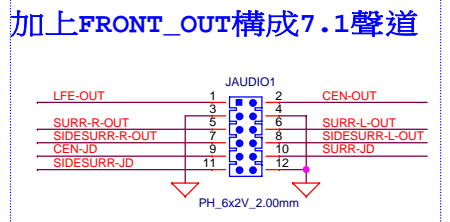
avalue Technology Inc.		Confidential	
Project Name EEV-EX14		Module Number IO-04	
Date Monday, September 23, 2013		Sheet 3 of 23	
Rev A0	Rev A11		Rev A11
Title USB2.0(0-5) · USB3.0(0-3)			

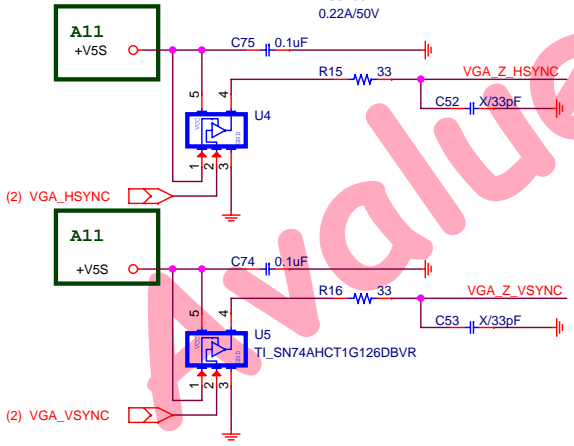
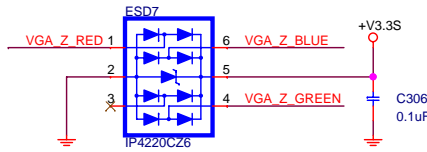
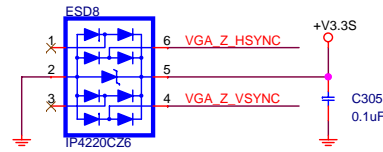
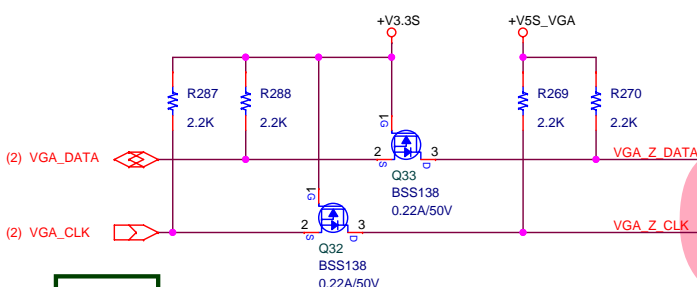
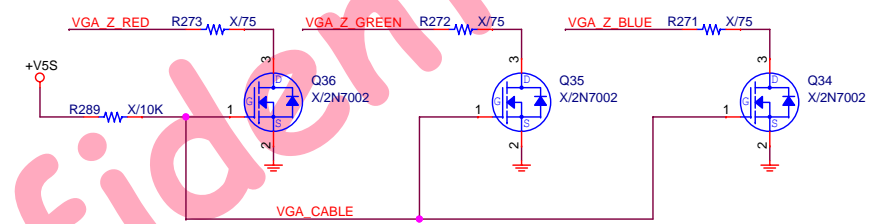
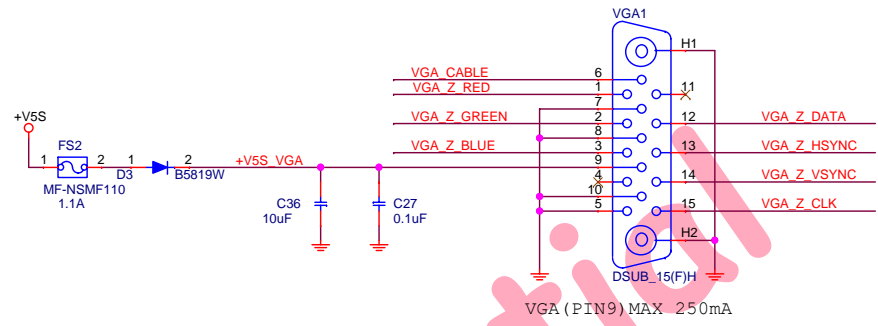
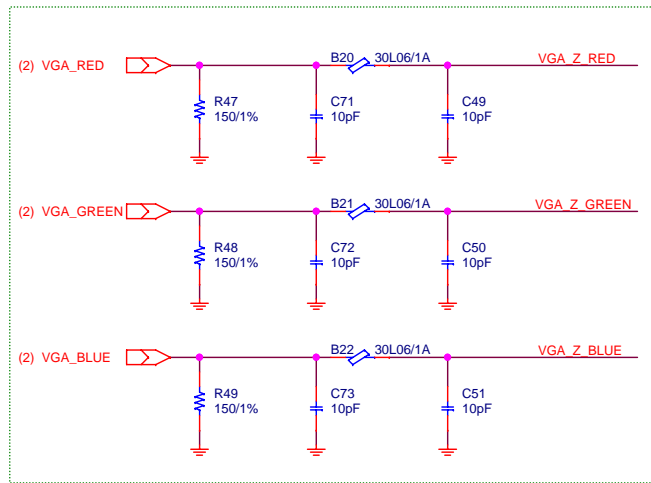
HD Audio(ALC892)

Sense:
 PortA(39,41):SenseA,39.2K
 PortB(21,22):SenseA,20K
 PortC(23,24):SenseA,10K
 PortD(35,36):SenseA,5.1K
 PortE(14,15):SenseB,39.2K
 PortF(16,17):SenseB,20K
 PortG(43,44):SenseB,10K
 PortH(45,46):SenseB,5.1K

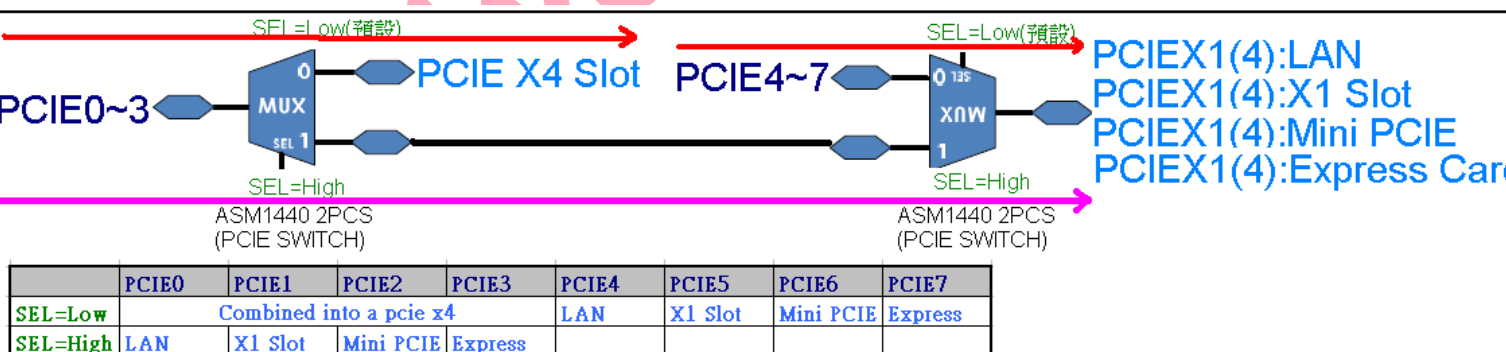
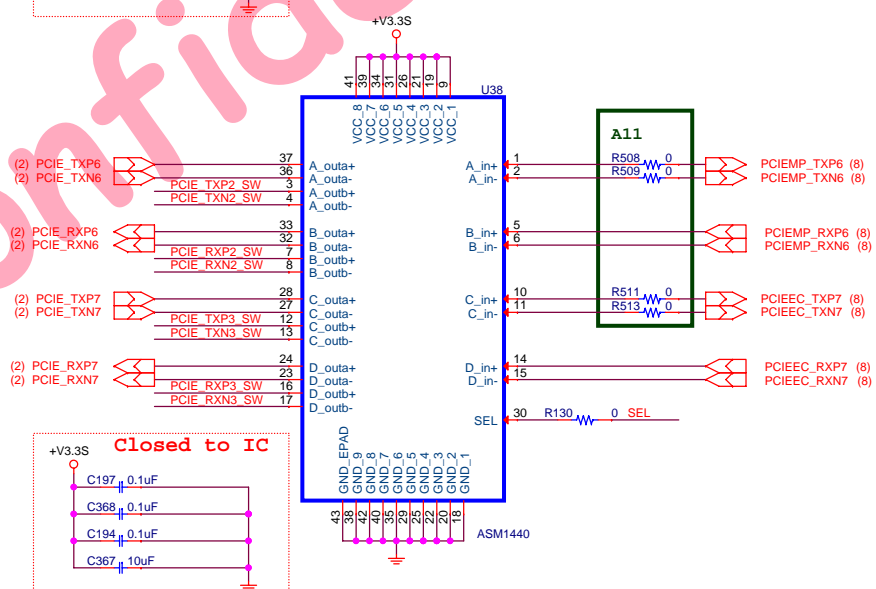
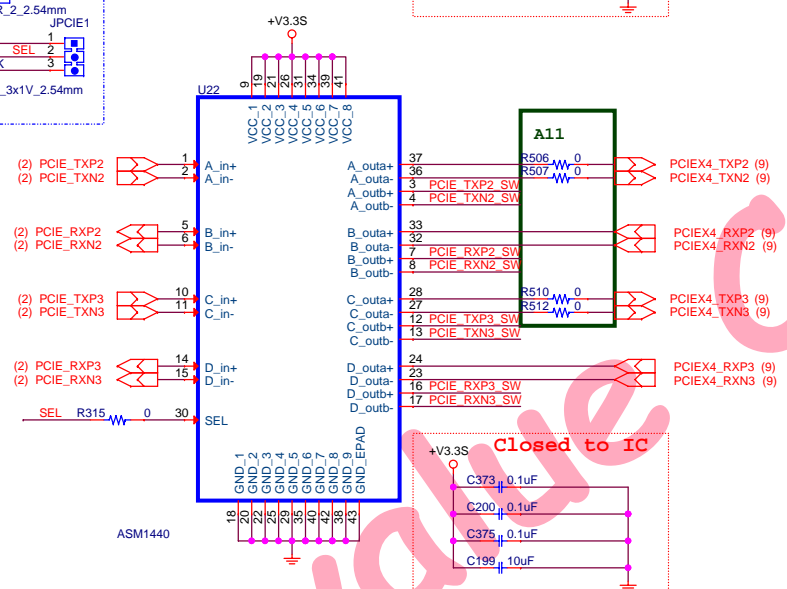
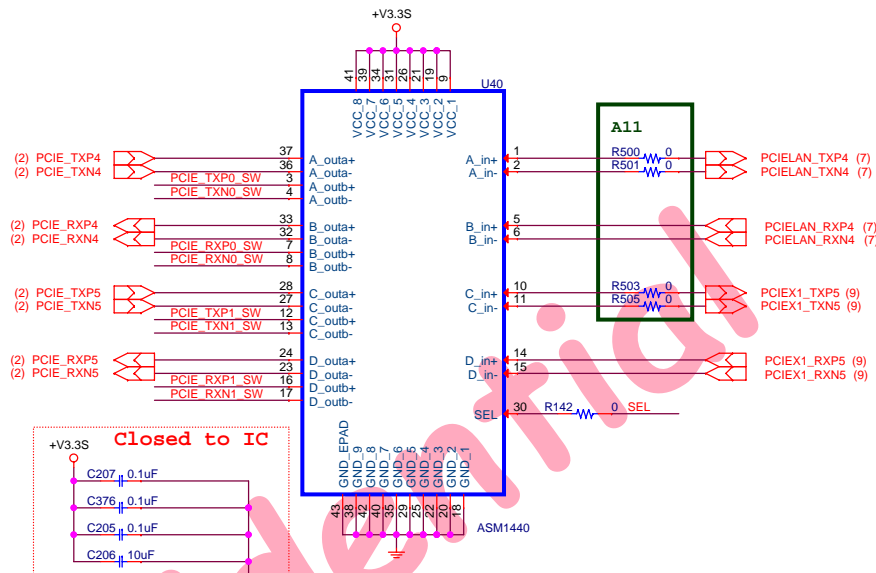
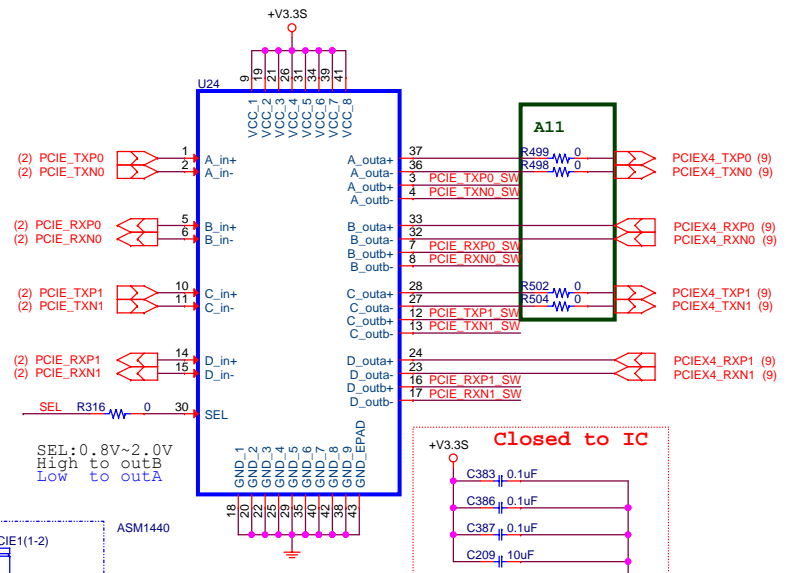


此 2 Connector有做小板可測試

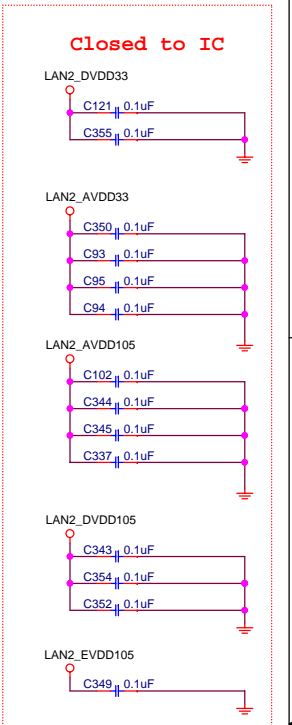
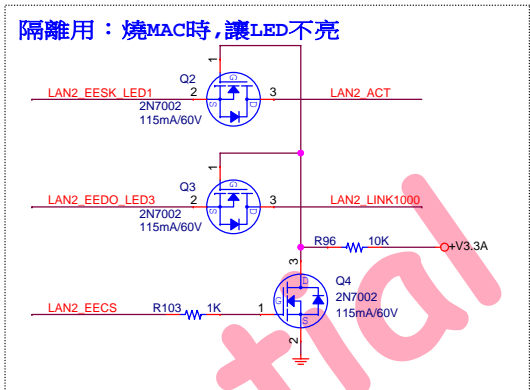
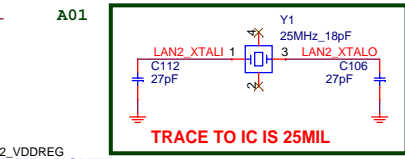
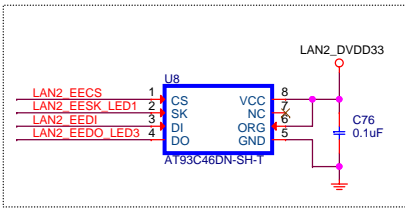
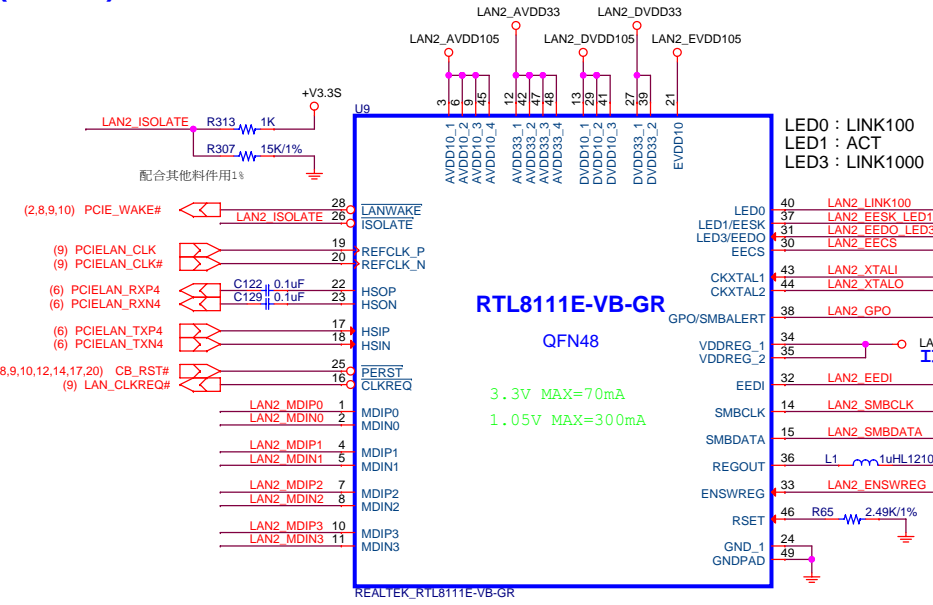




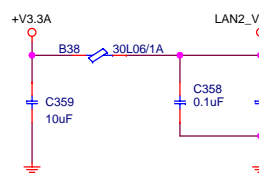
a value Technology Inc.		Confidential	
Project Name EEV-EX14		Module Number DSP-08	
Rev A01			
Size B	Title VGA		Rev A11
Date: Monday, September 23, 2013	Sheet 5	of 23	



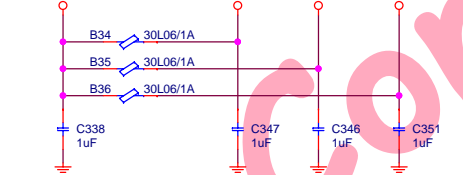
Carrier Board LAN IC (LAN2)



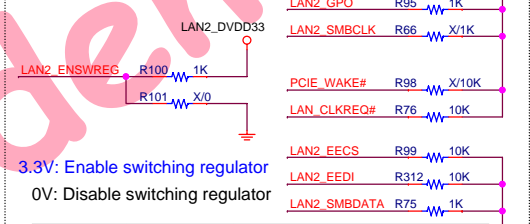
For Regulator Input



Regulator output



Strapping

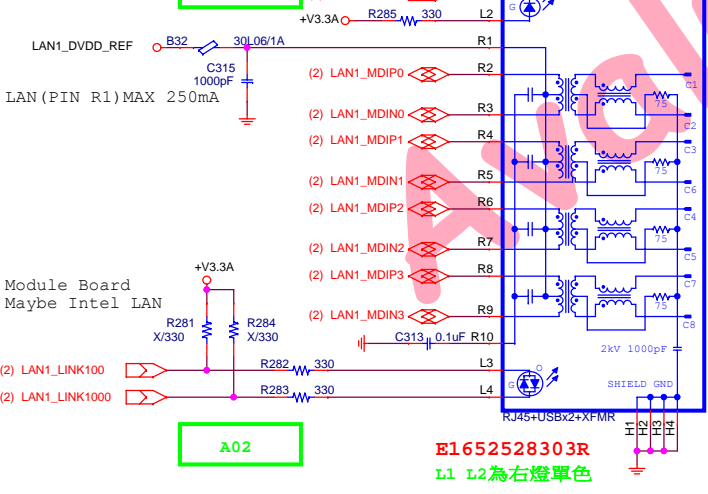


3.3V: Enable switching regulator
0V: Disable switching regulator

pin number	net name	Function	0	1
15	SMBDATA	ROM size	46	56 / 66
32	EEDI	TWSI/ROM	EEPROM	TWSI
33	LAN1_ENSR	Internal regulator	Disable	Enable

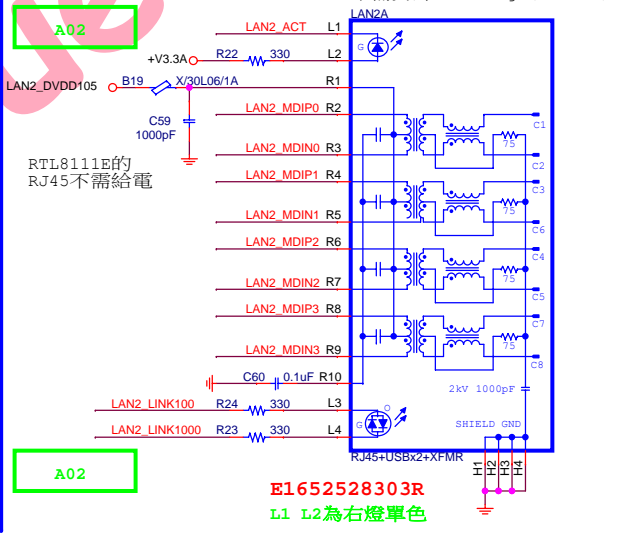
LAN1 Connector

給不給電 由上板LAN CHIP 決定
且電是由上板提供
INTEL為1.9V
RELTEK為1.05V



LAN2 Connector

LAN1~LAN2 A01
RTL8111E LED0、3需為1組
不需另外Pull High (L3、L4)



LAN2 Connector

LAN LED Active

	single LED	Dual LED	
	(green)	(green)	(orange)
10M	Blinking	X	X
100M	always ON	always ON	X
1000M	always ON	X	always ON

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Project Name: **EVE-EX14** Module Number: **LAN-03** Rev: **A0**

Size: **A3** Title: **LAN1、LAN2(RTL8111E)** Rev: **A11**

Date: **Monday, September 23, 2013** Sheet: **7** of **23**

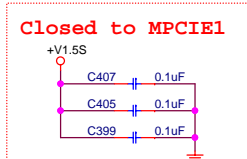
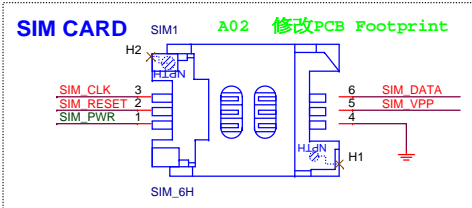
Mini_PCIE SLOT

PCB Footprint已改成非CIS
CIS有此料號, 但未含4個樞柱的孔
故請Layout修改完後另存成新的PCB Footprint
E1654252133R為H9.0高Connector

SIM library 有偏, 有再做調整成SIM_6P_254016MA006G100ZL_D

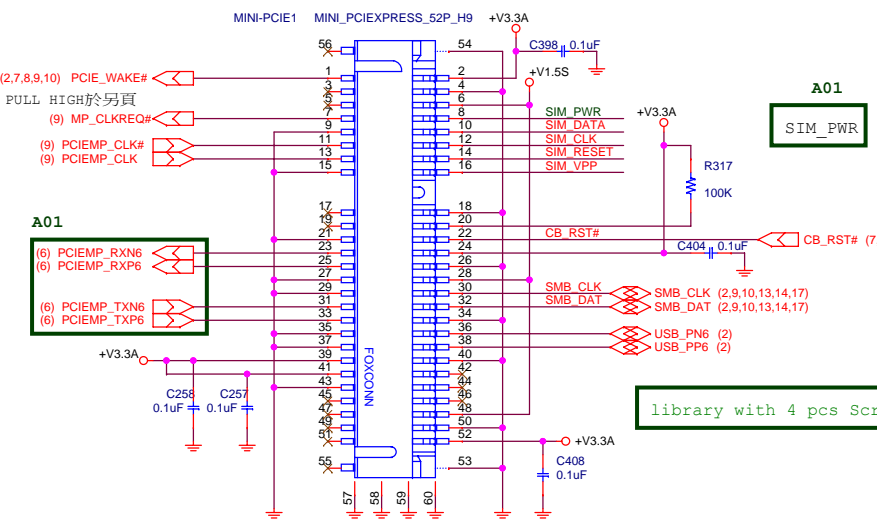
Mini PCI-E

Pin	Ver1.0	Ver1.2	Pin	Ver1.0	Ver1.2
1	WAKE#	WAKE#	2	+3.3V	+3.3Vaux
3	COEX1	COEX1	4	GND	GND
5	COEX2	COEX2	6	+1.5V	+1.5V
7	CLKREQ#	CLKREQ#	8	UIM_PWR	UIM_PWR
9	GND	GND	10	UIM_DATA	UIM_DATA
11	REFCLK-	REFCLK-	12	UIM_CLK	UIM_CLK
13	REFCLK+	REFCLK+	14	UIM_RESET	UIM_RESET
15	GND	GND	16	UIM_VPP	UIM_VPP
Mechanical Key					
17	UIM_C8	UIM_C8	18	GND	GND
19	UIM_C4	UIM_C4	20	W_DISABLE#	W_DISABLE#
21	GND	GND	22	PERST#	PERST#
23	PERn0	PERn0	24	+3.3Vaux	+3.3Vaux
25	PERp0	PERp0	26	GND	GND
27	GND	GND	28	+1.5V	+1.5V
29	GND	GND	30	SMB_LCK	SMB_LCK
31	PETn0	PETn0	32	SMB_DATA	SMB_DATA
33	PETp0	PETp0	34	GND	GND
35	GND	GND	36	USB_D-	USB_D-
37	Reserved	GND	38	USB_D+	USB_D+
39	Reserved	+3.3Vaux	40	GND	GND
41	Reserved	+3.3Vaux	42	LED_WWAN#	LED_WWAN#
43	Reserved	GND	44	LED_WLAN#	LED_WLAN#
45	Reserved	Reserved	46	LED_WPAN#	LED_WPAN#
47	Reserved	Reserved	48	+1.5V	+1.5V
49	Reserved	Reserved	50	GND	GND
51	Reserved	Reserved	52	+3.3V	+3.3Vaux

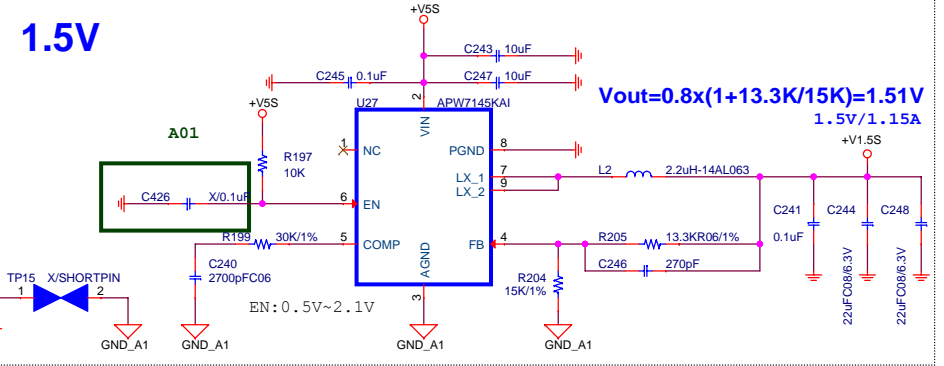
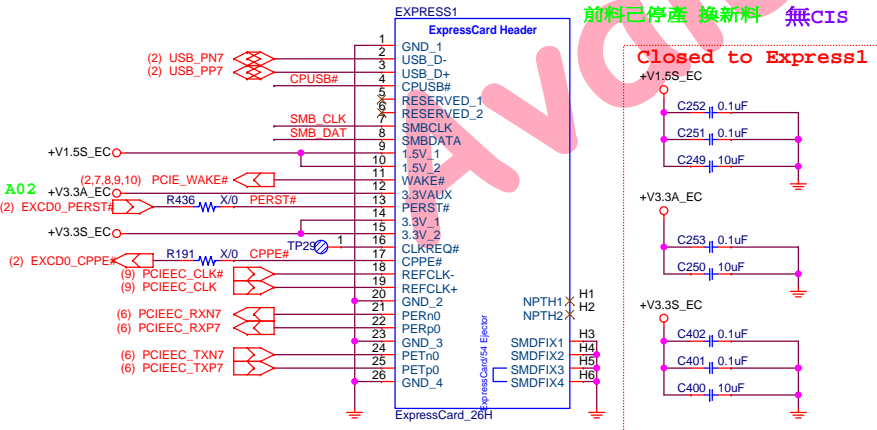
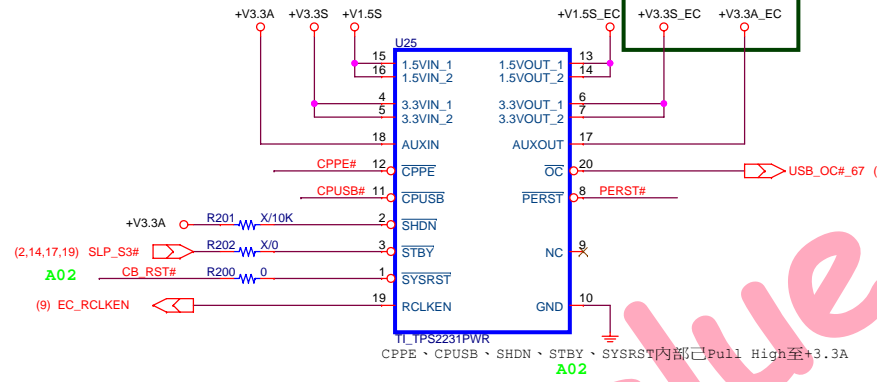


library with 4 pcs Screw holes(#1~#4)

Power	Voltage	Primary Power		Auxiliary Power
		Peak mA	Normal mA	Normal mA
+3.3Vaux	±9%	2750	1100	250(wake EN)
+1.5V	±5%	500	375	N/A
+1.5V	±5%	500	375	N/A



EXPRESS CARD



Supply	Limits ²
+3.3V ¹	1000 mA – Average 1300 mA – Max
+3.3VAUX ¹	250 mA – Average 275 mA – Max
+1.5V	5 mA – Average 500 mA – Average 650 mA – Max

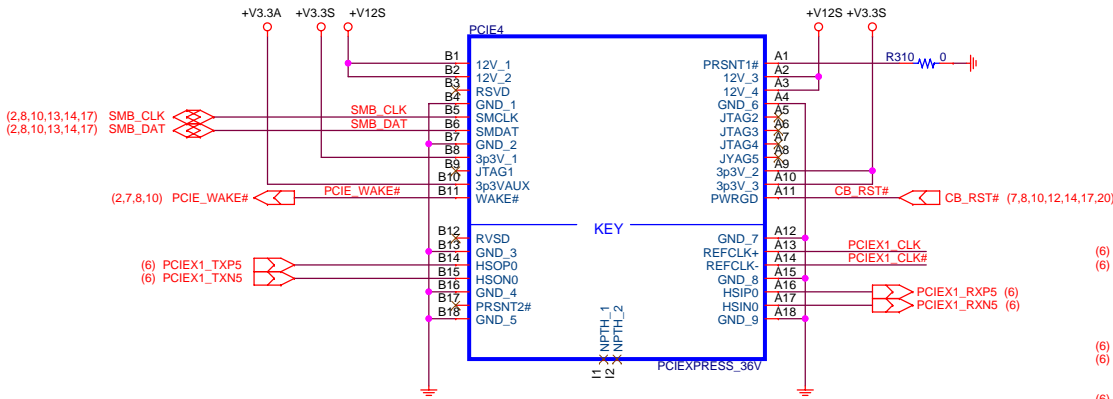
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Project Name: **EEV-EX14** | Module Number: **SLT-04** | Rev: **A1**

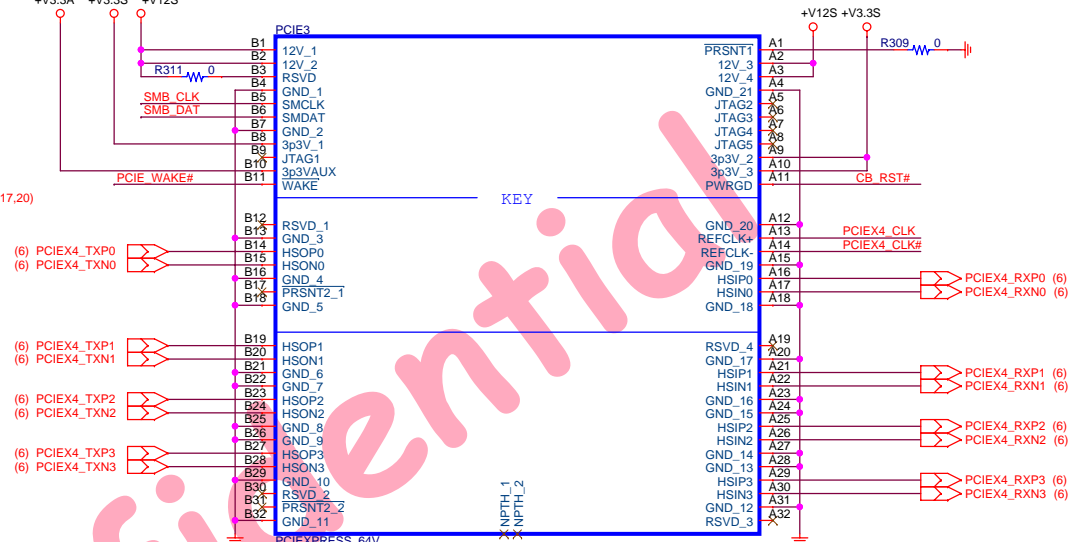
Size: **A3** | Title: **MINI PCI-E CARD - EXPRESS CARD** | Rev: **A11**

Date: **Monday, September 23, 2013** | Sheet: **8** of **23**

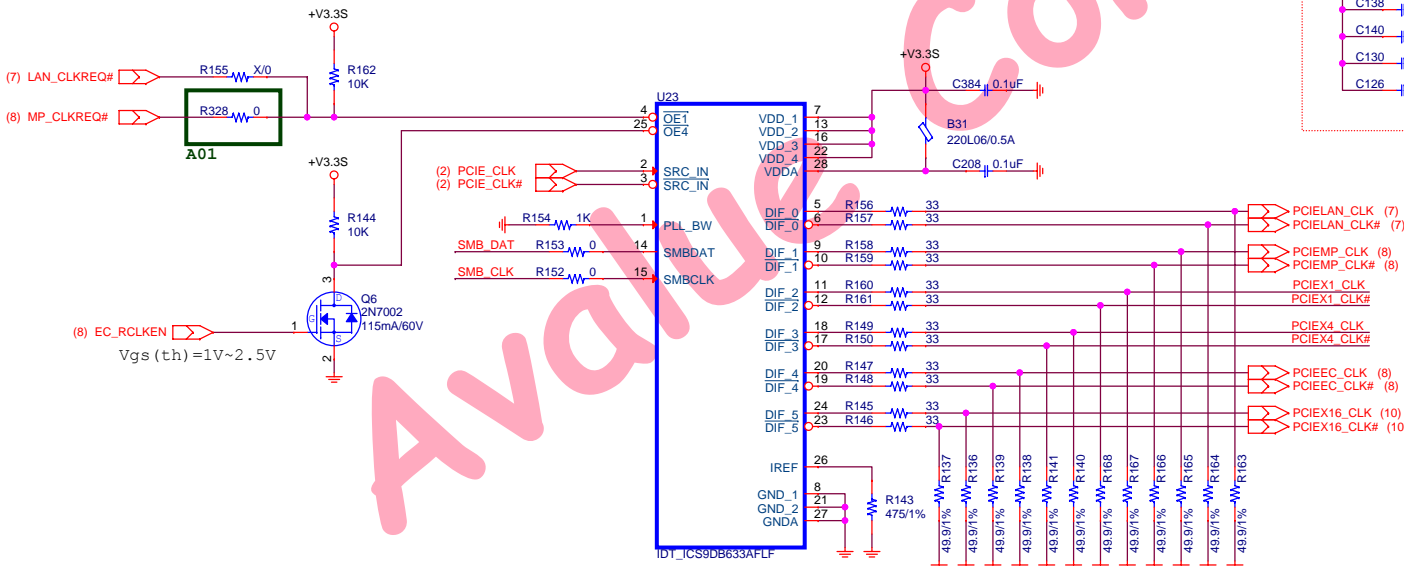
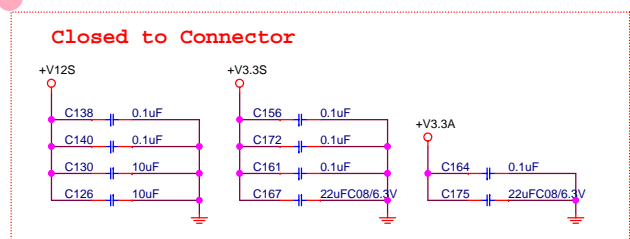
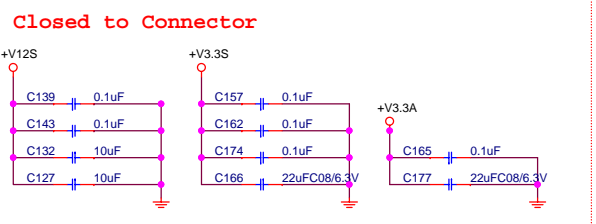
PCIE X1 SLOT



PCIE X4 SLOT



参考COM Expree Datasheet
X1 JTAG ALL NC
PIN B3: Only PCIE X4 X16 Link 12V
PIN A11: Define PERST#
PIN A1、B17用法: 支援電源熱插拔用
A1 接GND, B17 Pull High,
CARD Device會將此2pin相連,
故底板B17就可控制電源輸出或通知BIOS

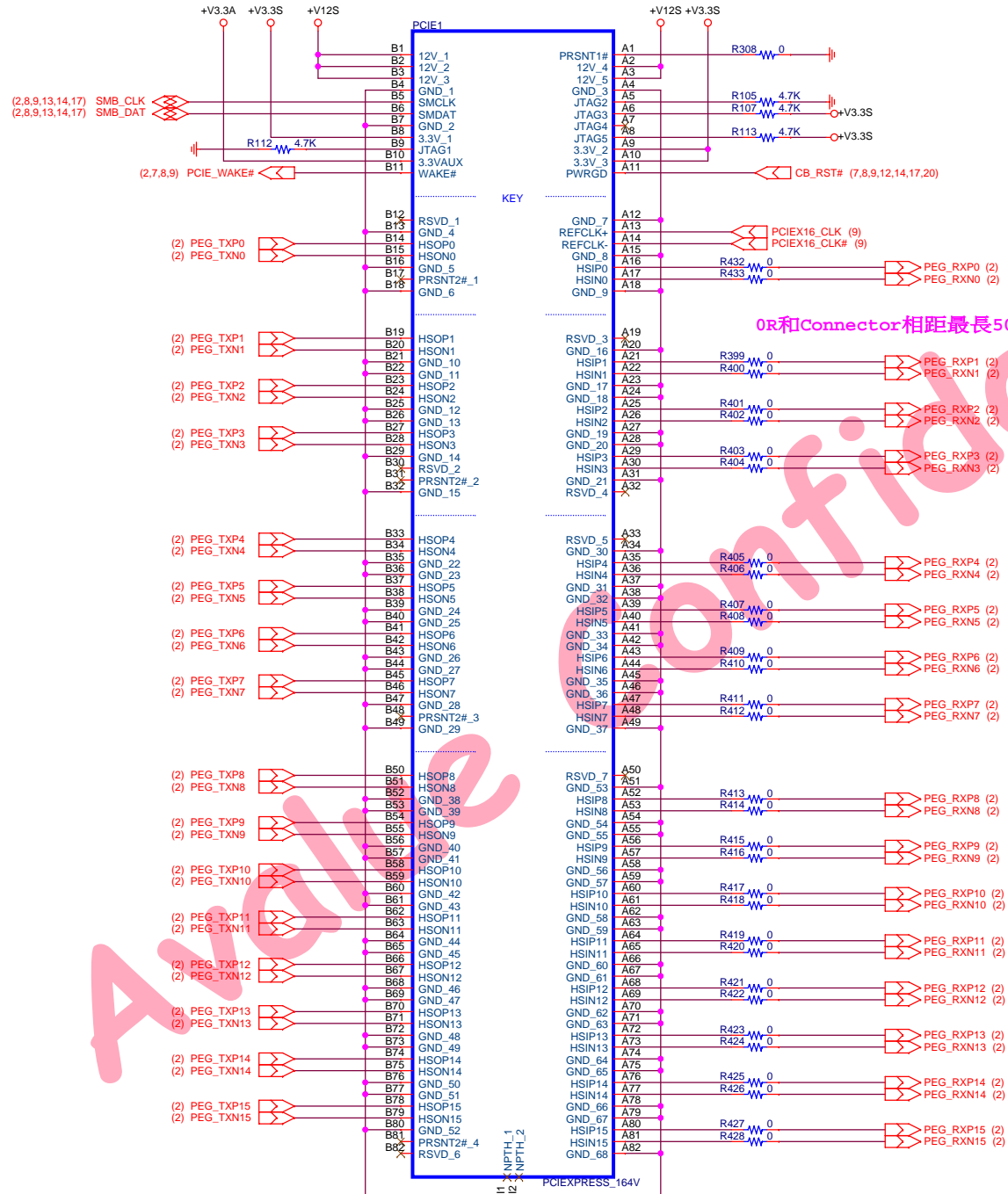


33及49.9均不需用1%

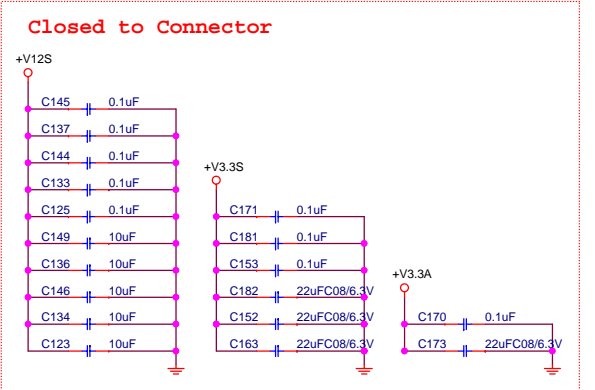
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Project Name	EEV-EX14	Module Number	<Module no.>	Rev	?
Size	A3	Title	PCIE X1、PCIE X4 - CLOCK BUFFER	Rev	A11
Date:	Monday, September 23, 2013	Sheet	9	of	23

参考COM Expree Datasheet
 X16 JTAG 接法如下
 PIN B3: Only PCIE X4 X16 Link 12V
 PIN A11: Define PERST#



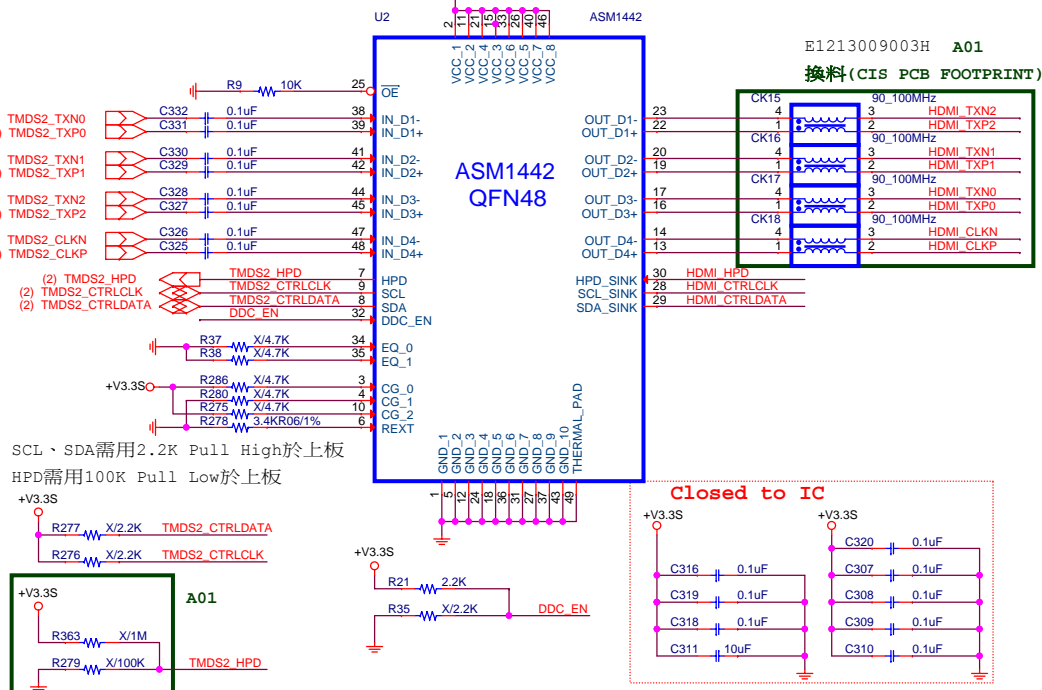
0R和Connector相距最長500mils



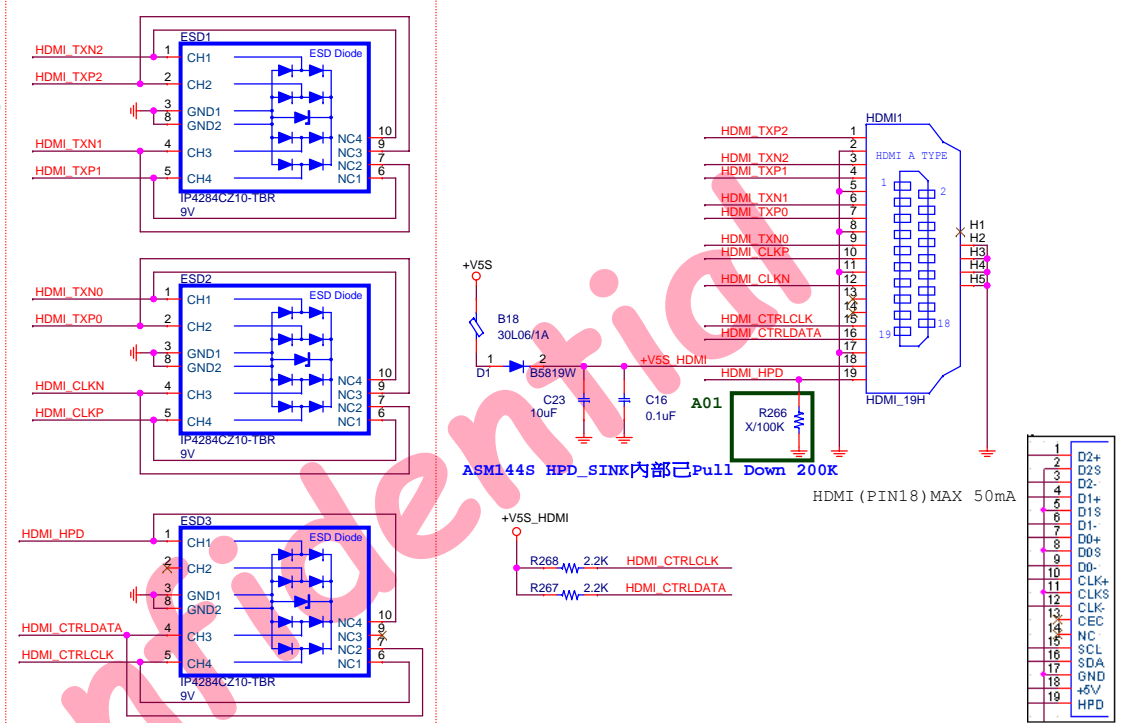
avalue Technology Inc.		Confidential	
Project Name	EEV-EX14	Module Number	<Module no.>
Size	A3	Rev	?
Title	PCIEX16	Rev	A11
Date:	Monday, September 23, 2013	Sheet	10 of 23

HDMI Connector

0~3組差動訊號0.1uF加於下板

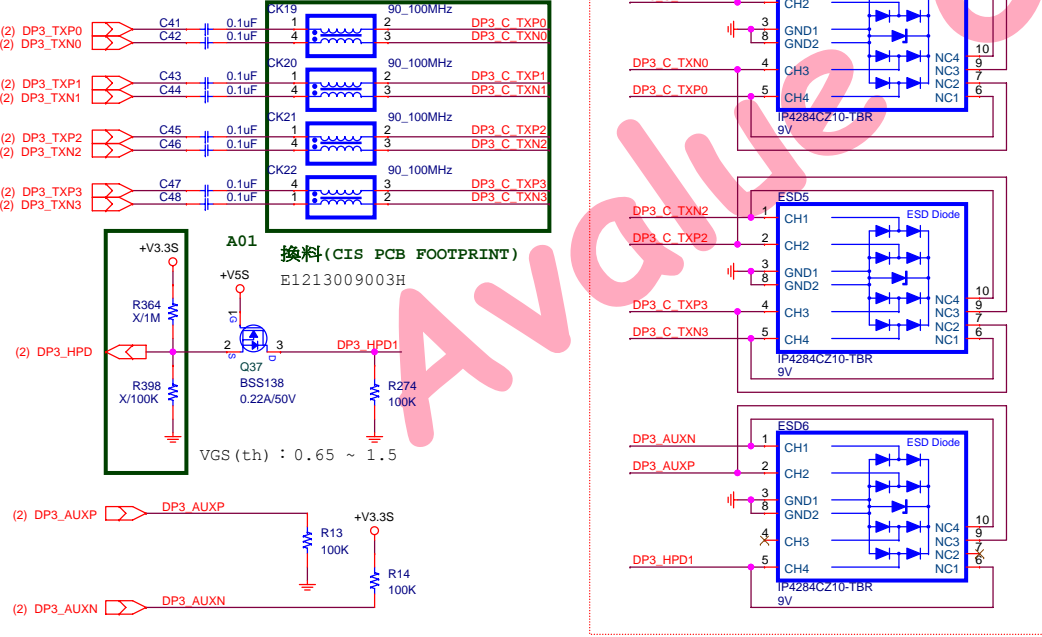


Closed to Connector

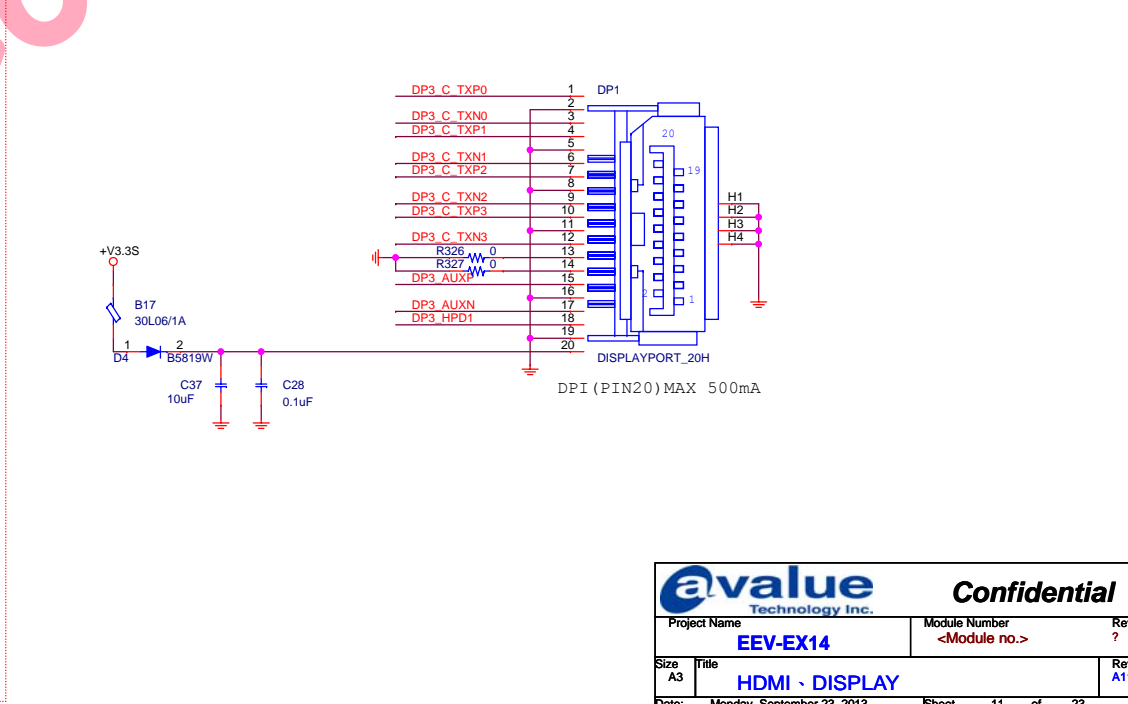


Display Connector

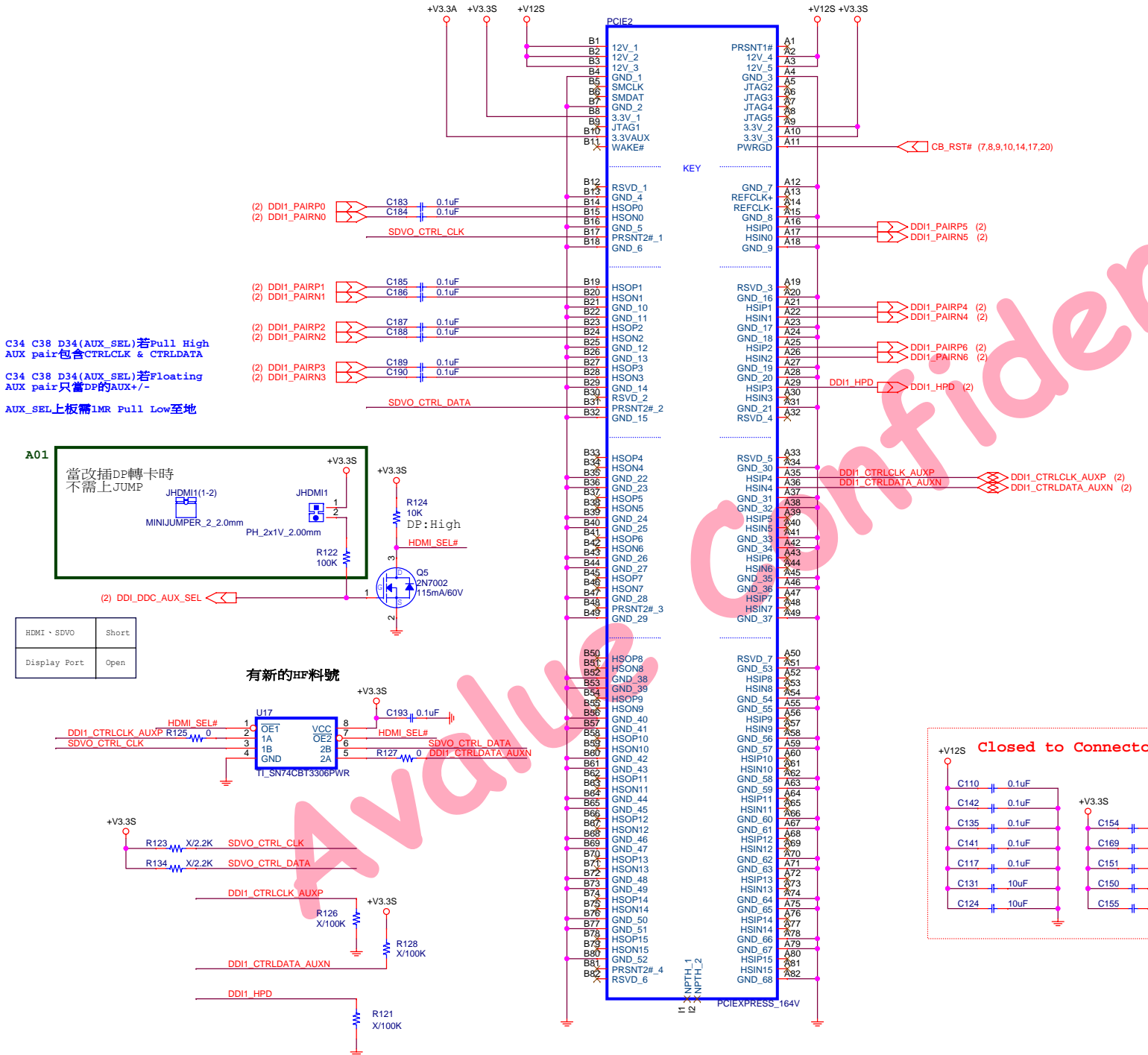
0~3組差動訊號0.1uF加於下板



Closed to Connector



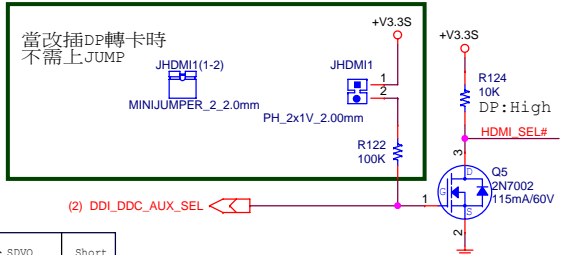
ADD2N CARD SLOT
料號改過：藍色SLOT



C34 C38 D34(AUX_SEL)若Pull High
AUX pair包含CTRLCLK & CTRLDATA

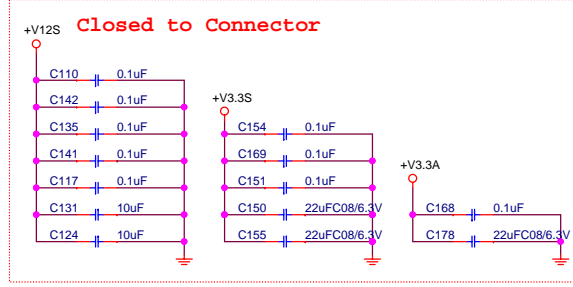
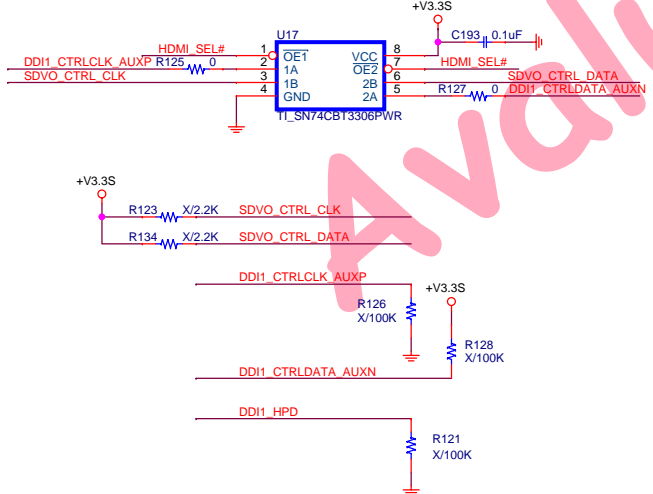
C34 C38 D34(AUX_SEL)若Floating
AUX pair只當DP的AUX+/-

AUX_SEL上板需1MR Pull Low至地



HDMI - SDVO	Short
Display Port	Open

有新的IC料號

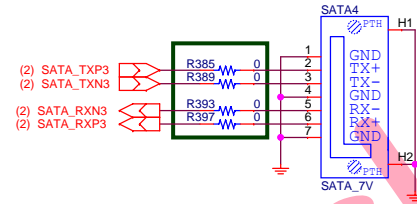
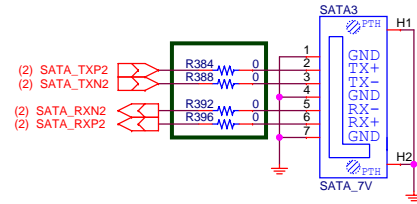
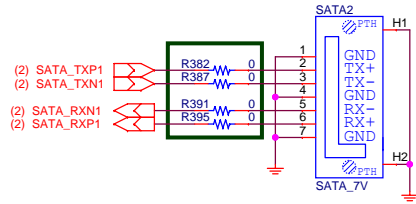
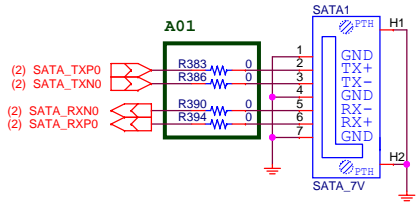


Pin Name	Type 6 Pin Number	SDVO	DP	HDMI/DVI (TMDS Signaling)
DDI1_PAIR0+	D26	SDVO1_RED+	DP1_LANE0+	TMDS1_DATA2+
DDI1_PAIR0-	D27	SDVO1_RED-	DP1_LANE0-	TMDS1_DATA2-
DDI1_PAIR1+	D29	SDVO1_GRN+	DP1_LANE1+	TMDS1_DATA1+
DDI1_PAIR1-	D30	SDVO1_GRN-	DP1_LANE1-	TMDS1_DATA1-
DDI1_PAIR2+	D32	SDVO1_BLU+	DP1_LANE2+	TMDS1_DATA0+
DDI1_PAIR2-	D33	SDVO1_BLU-	DP1_LANE2-	TMDS1_DATA0-
DDI1_PAIR3+	D36	SDVO1_CK+	DP1_LANE3+	TMDS1_CLK+
DDI1_PAIR3-	D37	SDVO1_CK-	DP1_LANE3-	TMDS1_CLK-
DDI1_PAIR4+	C25	SDVO1_INT+		
DDI1_PAIR4-	C26	SDVO1_INT-		
DDI1_PAIR5+	C29	SDVO1_TVCLKIN+		
DDI1_PAIR5-	C30	SDVO1_TVCLKIN-		
DDI1_PAIR6+	C15	SDVO1_FLDSTALL+		
DDI1_PAIR6-	C16	SDVO1_FLDSTALL-		
DDI1_HPDP	C24		DP1_HPDP	HDMI1_HPDP
DDI1_CTRLCLK_AUX+	D15	SDVO1_CTRLCLK	DP1_AUX+	HDMI1_CTRLCLK
DDI1_CTRLDATA_AUX-	D16	SDVO1_CTRLDATA	DP1_AUX-	HDMI1_CTRLDATA
DDI1_DDC_AUX_SEL	D34			

SATA1~4

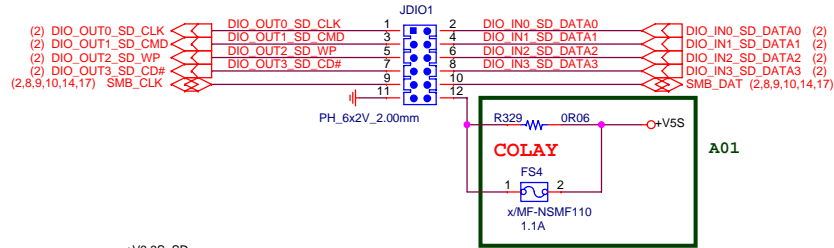
TX RX 電容 均應加於上板

0R和SATA Connector相距最長100mils

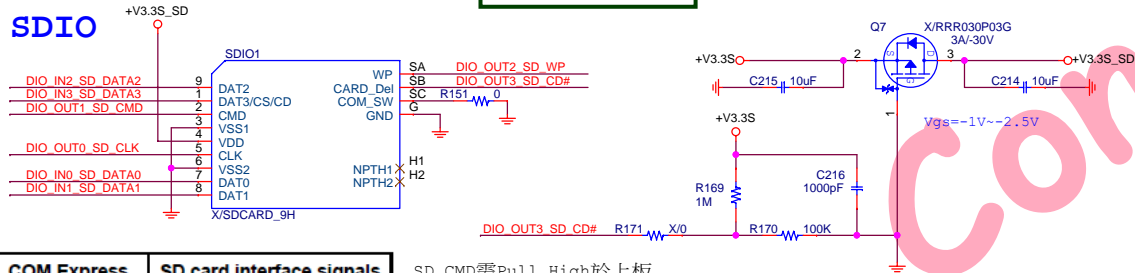


DIO (4IN/4OUT)

上板決定為:DIO功能或SDIO功能



SDIO

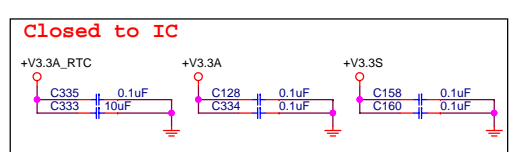
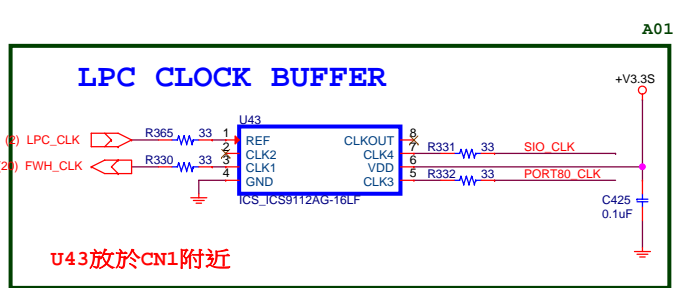
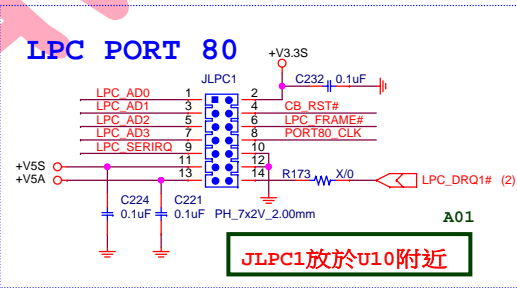
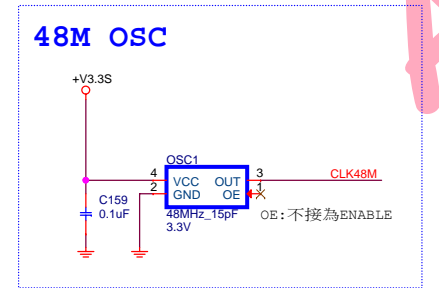
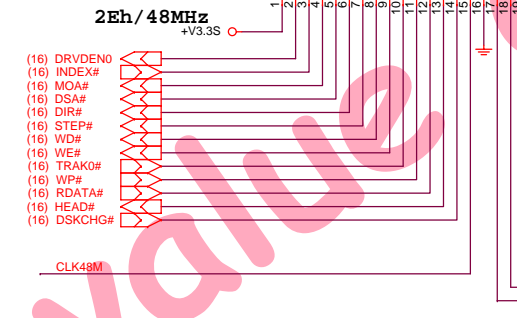
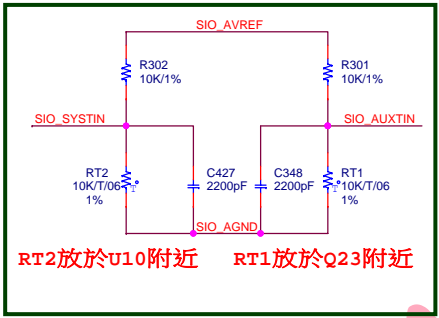
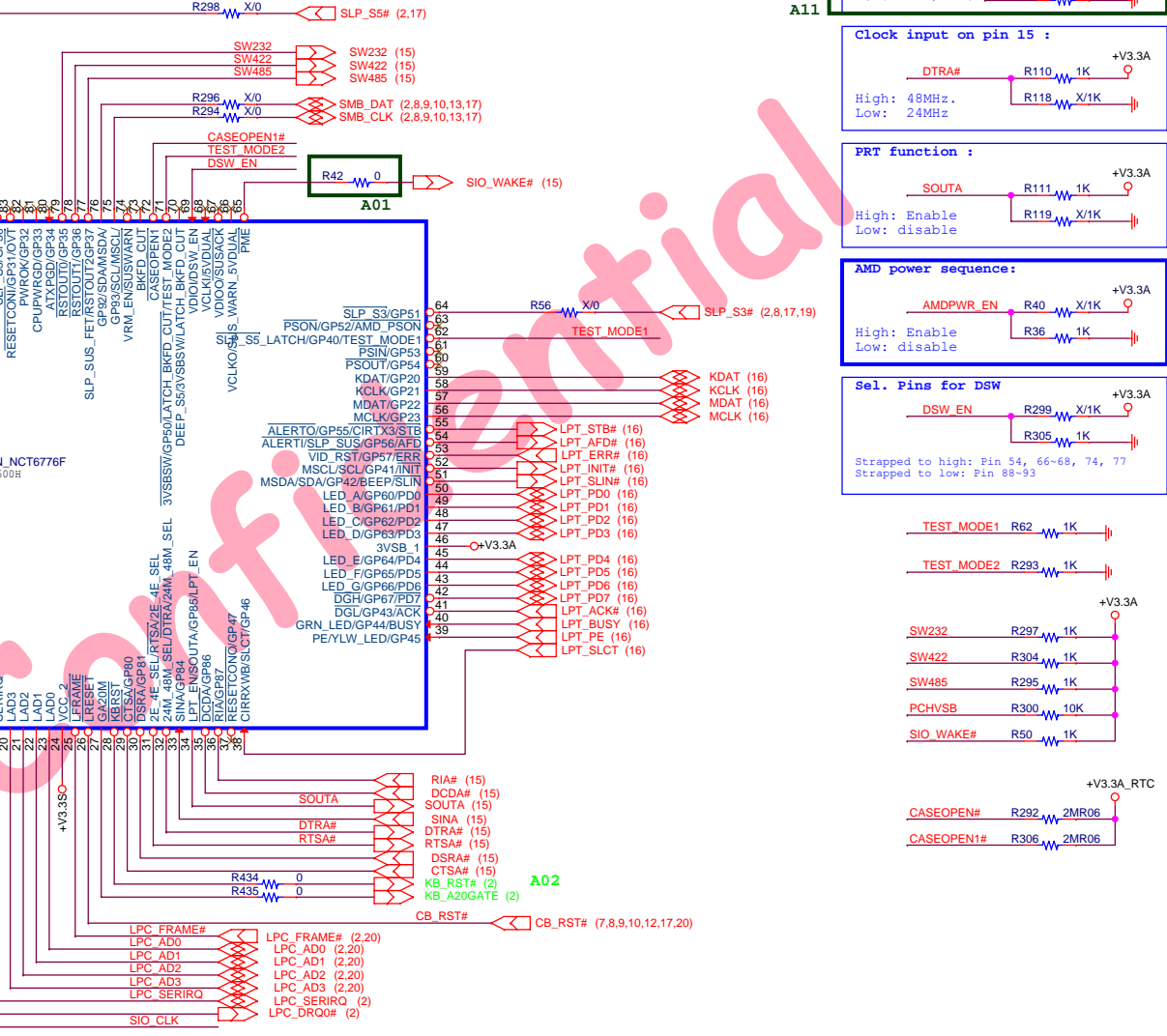
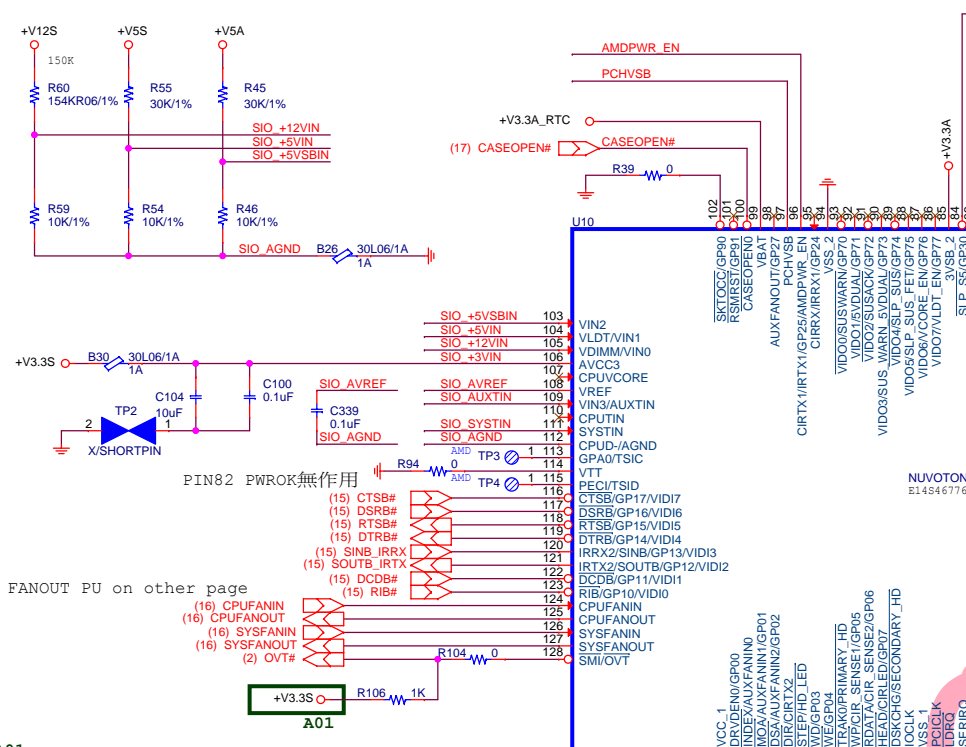
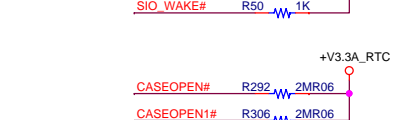
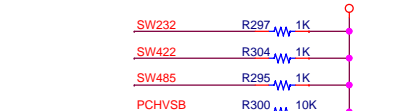
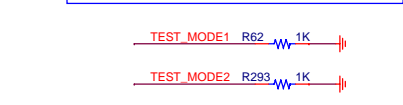
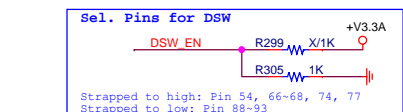
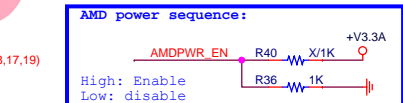
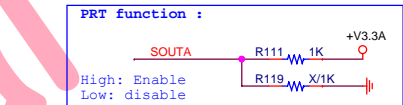
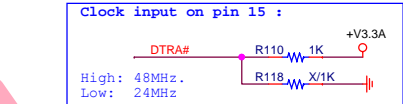
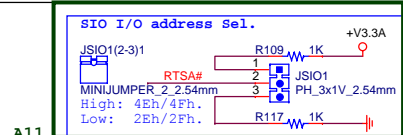


SD_CMD需Pull High於上板
SD_WP 需Pull High於上板
SD_CD#需Pull High於上板

COM Express Signal	SD card interface signals
GPI0	SD_DATA0
GPI1	SD_DATA1
GPI2	SD_DATA2
GPI3	SD_DATA3
GPO0	SD_CLK
GPO1	SD_CMD
GPO2	SD_WP
GPO3	SD_CD#

Card detection switch		Write protection switch			
When card is ejected	When card is inserted	When card is ejected	When card is inserted		
			Write protect	Write enable	
OPEN	CLOSE	OPEN	OPEN	CLOSE	
Sb Sc	Sb Sc	Sa Sc	Sa Sc	Sa Sc	Sa Sc

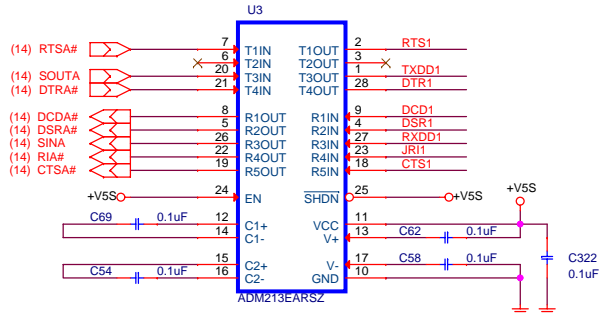
**因客戶的底板很有可能不使用Super I/O
故目前設計不使用ACPI功能**



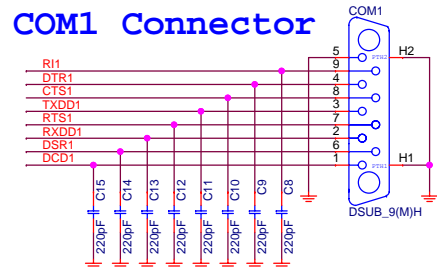
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Project Name		Module Number	Rev
EEV-EX14		<Module no.>	?
Size A3	Title	Rev	
	SUPER I/O(NCT6776F)	A11	
Date:	Monday, September 23, 2013	Sheet	14 of 23

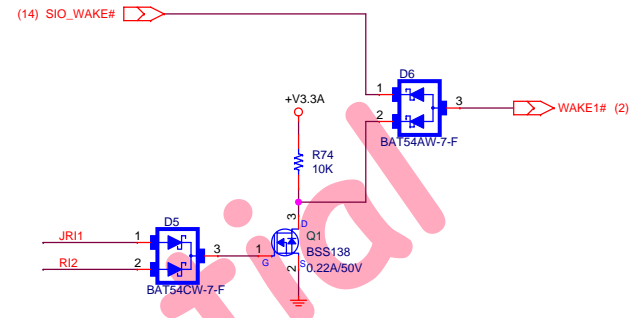
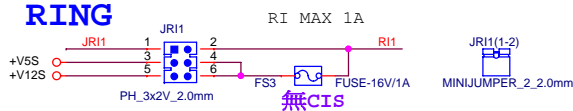
COM1



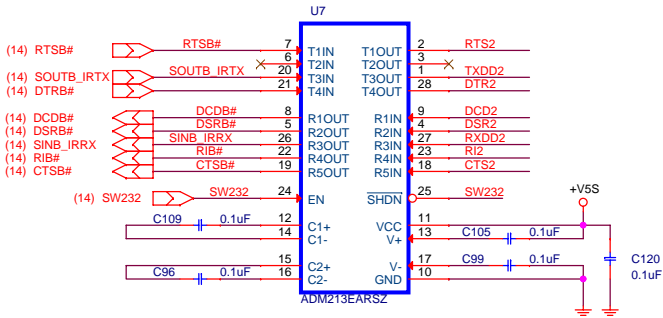
COM1 Connector



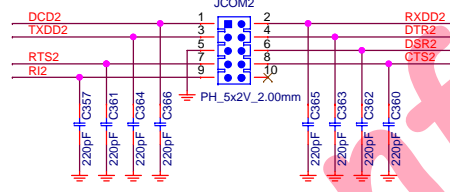
RING



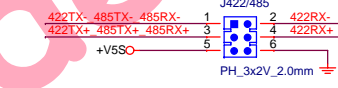
COM2



COM2 Connector

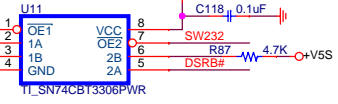


RS485/422 Connector

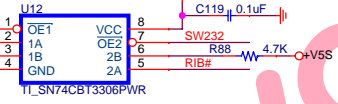


	PIN1	PIN2	PIN3	PIN4
RS422	TX-	RX-	TX+	RX+
RS485	TX-		TX+	

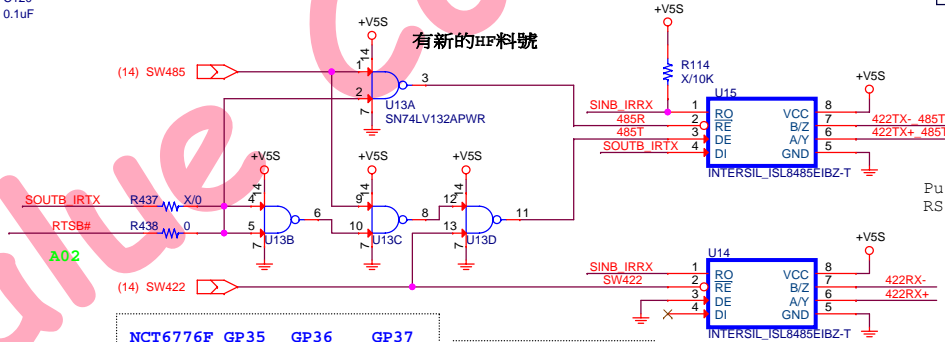
有新的HF料號



有新的HF料號



有新的HF料號



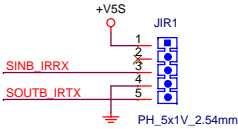
Pull High及Pull Low為 RS485 Mode自動接收用

	NCT6776F	GP35	GP36	GP37
GPIO:	SW232	SW422	SW485	
RS232:	<HI>	HI	LO	
RS422:	LO	<LO>	LO	
RS485:	LO	HI	<HI>	
IR :	LO	HI	LO	

SN74LV132APWRG4		
A	B	Y
H	H	L
L	X	H
X	L	H

RS485 Mode			
SOUTB_IRTX	485R	485T	
L	H	H	
H	L	L	

IR



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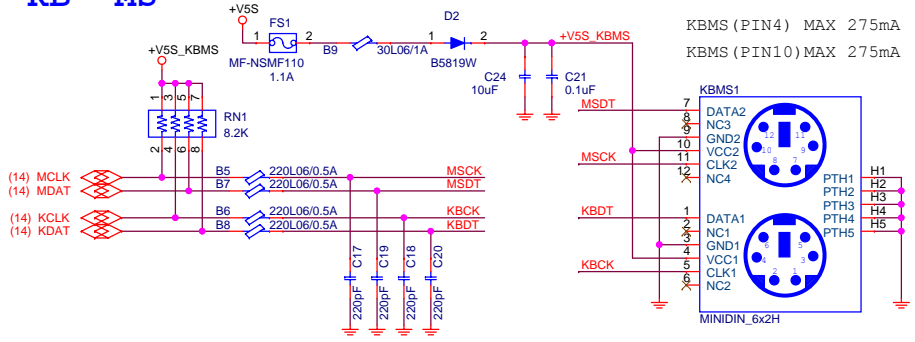
Project Name: **EEV-EX14** Module Number: <Module no.> Rev ?

Date: Monday, September 23, 2013 Sheet 15 of 23

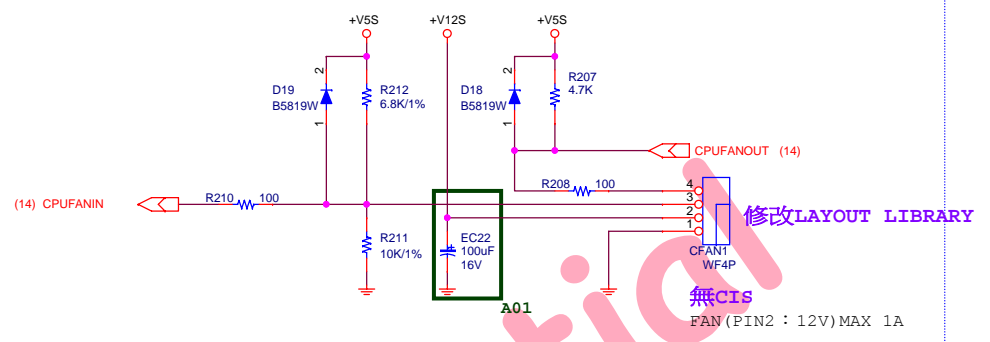
Size A3 Title: **COM1 · COM2** Rev A11

KB、MS

KB、MS Connector

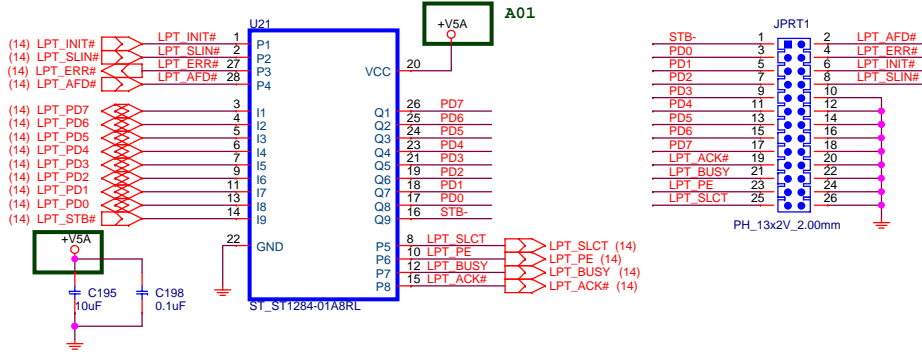


CPUFAN0

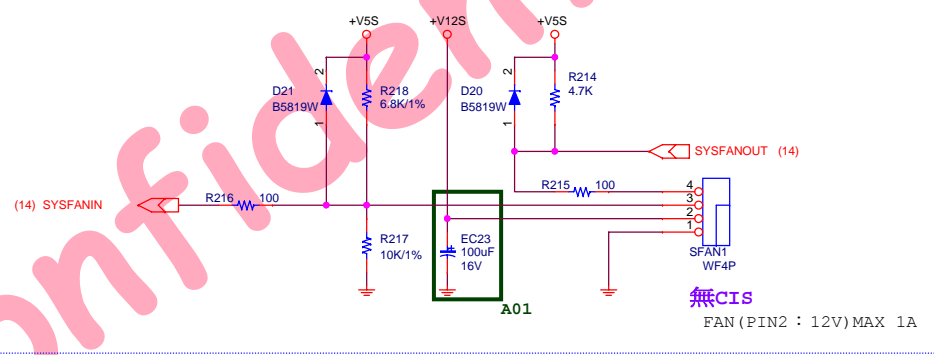


PRINTER (PRT)

PRINTER Connector

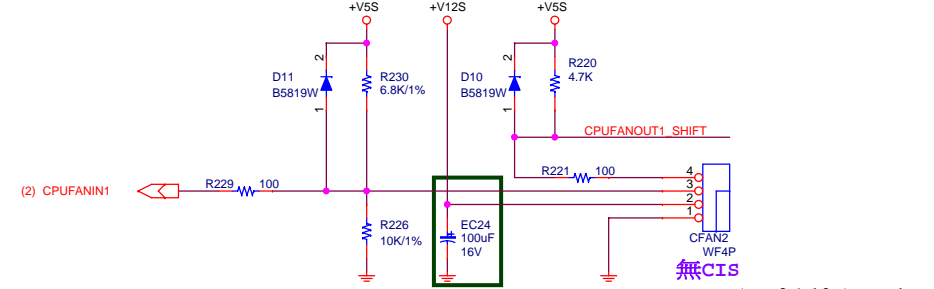
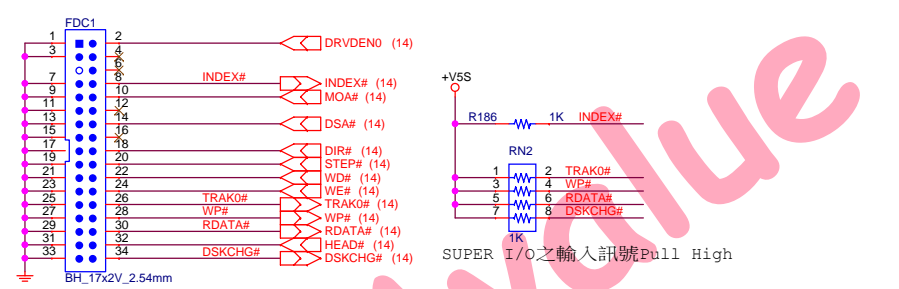


SYSFAN0

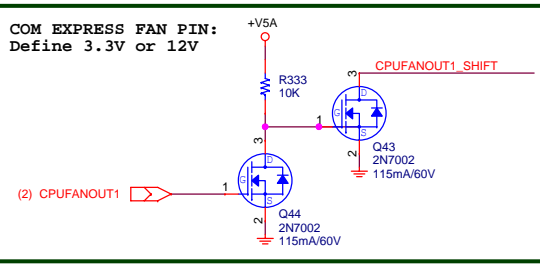
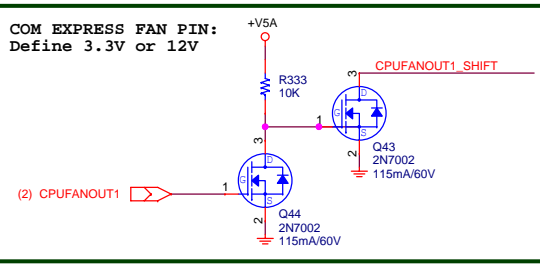


FLOPPY Connector (FDC)

CPUFAN1

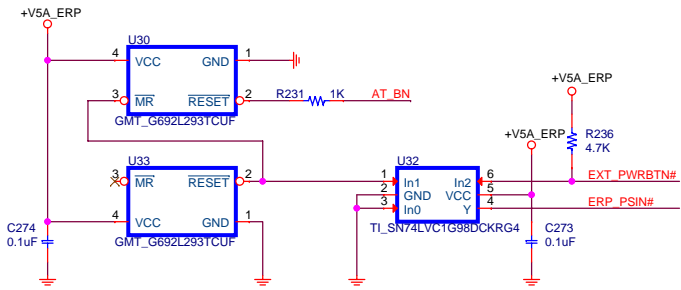


BATTERY



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Project Name	EEV-EX14	Module Number	<Module no.>
Rev	?	Rev	?
Size	A3	Title	KB、MS、PRT、FDC、BAT、FAN
Date:	Monday, September 23, 2013	Sheet	16 of 23

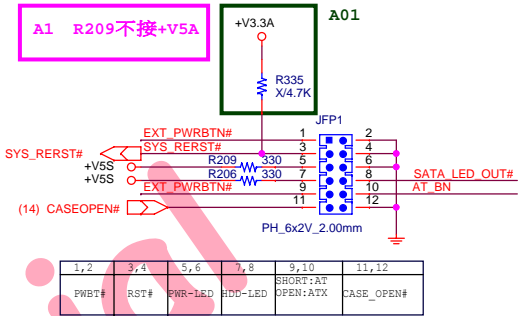
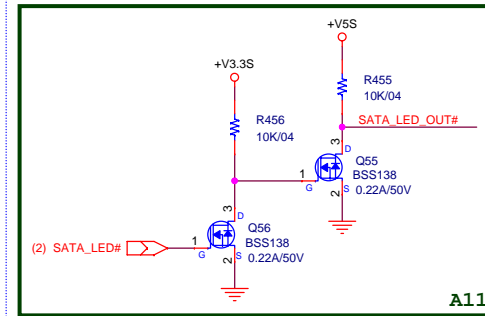
AUTO POWER ON



SN74LVC1G98

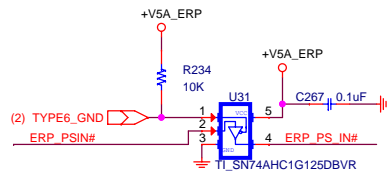
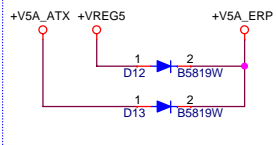
In2(6)	In1(1)	In0(3)	Y(4)
L	L	L	H
L	H	L	L
H	H	L	H
H	L	L	H

FRONT PANEL

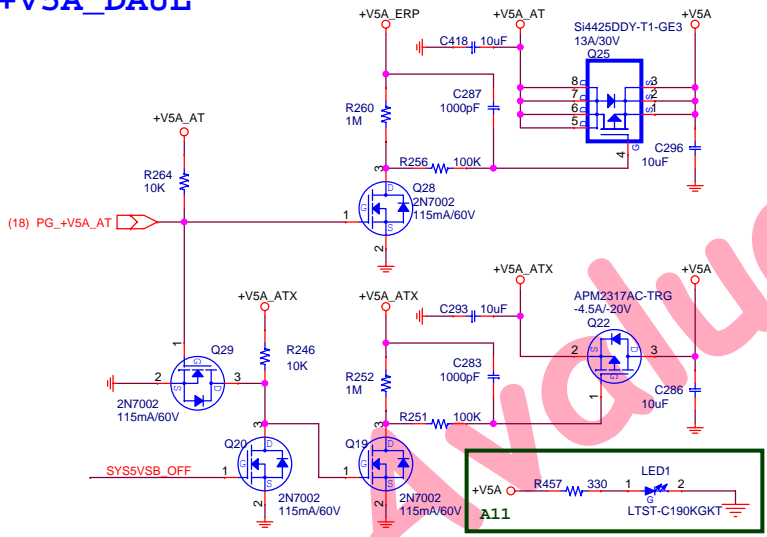


因Erp有限制要低於0.5W
故需控制此3個電源的使用

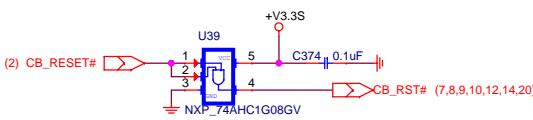
TYPE6_GND於上板接地



+V5A_DUAL



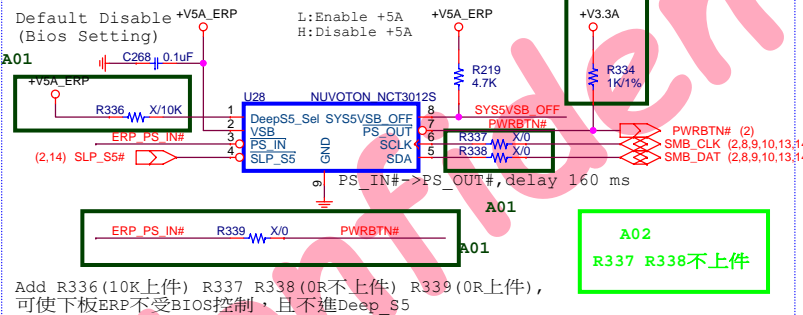
RESET BUFFER



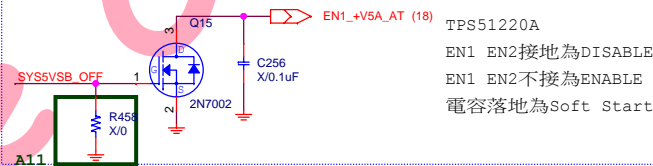
SN74AHC1G08

A	B	Y
H	H	H
L	X	L
X	L	L

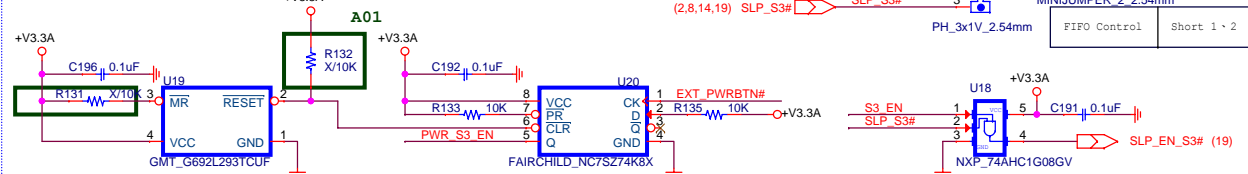
ErP



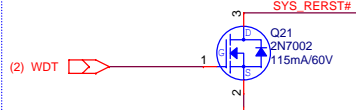
EN1: +V5A_AT



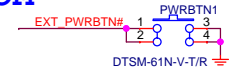
防止第一次開機S3為High而使電源轉出



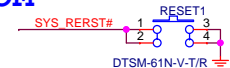
WDT



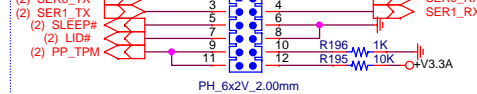
POWER BUTTON



RESET BUTTON



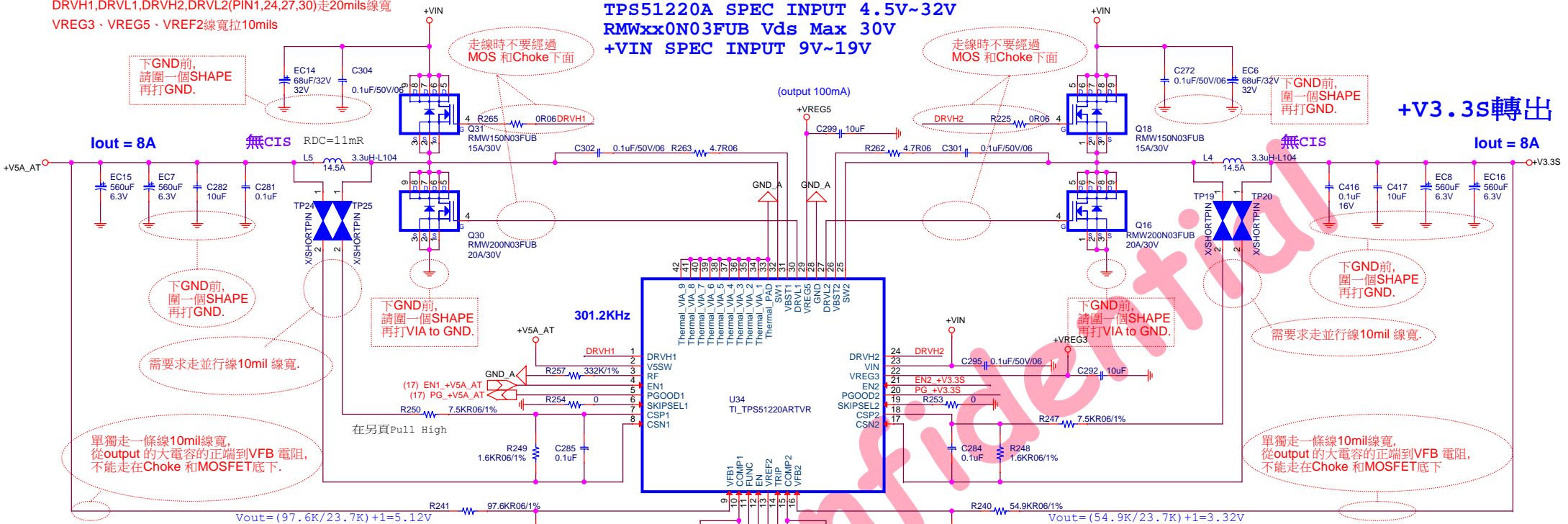
RESET BUTTON



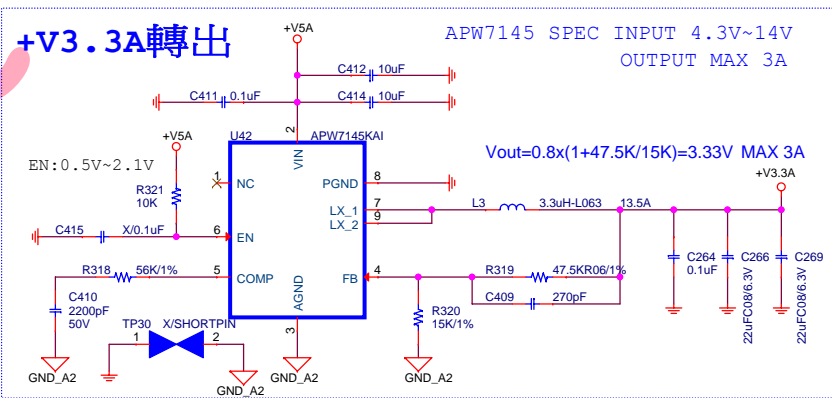
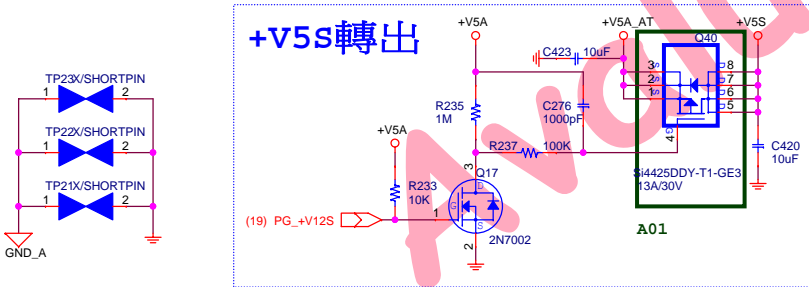
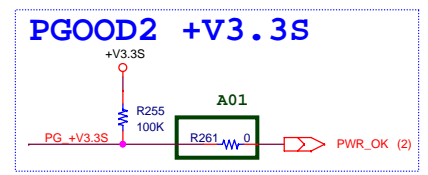
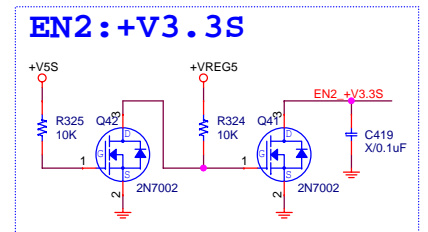
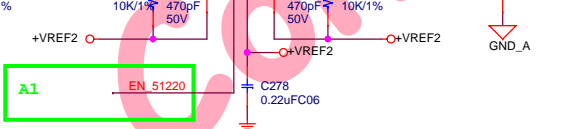
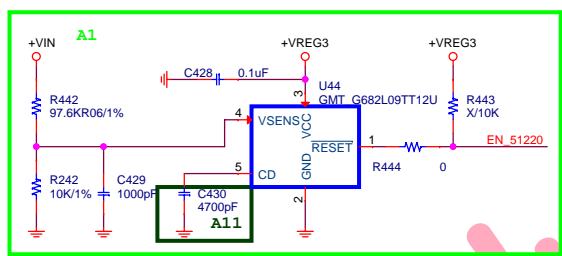
DRVH1,DRV1,DRVH2,DRV2(PIN1,24,27,30)走20mil線寬
VREG3、VREG5、VREF2線寬拉10mil

TPS51220A SPEC INPUT 4.5V~32V
RMWxx0N03FUB Vds Max 30V
+VIN SPEC INPUT 9V~19V

+V3.3S轉出



$V_{out} = (97.6K / 23.7K) + 1 = 5.12V$ $V_{out} = (54.9K / 23.7K) + 1 = 3.32V$



SKIPSEL (PIN6 19)

GND	Continuous conduction mode
VREG2	Auto Skip
VREG3	Auto Skip, maximum 7 skip (suitable for FSW < 400KHz)
VREG5	Auto SKIP, maximum 15 skip (suitable for equal to or greater than 400KHz)

FUNC (PIN11)
GND: Current mode, OVP enable
VREF2: D-CAP mode, OVP disable
VREG3: D-CAP mode, OVP enable
VREG5: Current mode, OVP disable

Overcurrent trip level and discharge mode TRIP (PIN14)
GND: V(OCL-ULV), discharge on
VREF2: V(OCL-ULV), discharge off
VREG3: V(OCL-LV), discharge off
VREG5: V(OCL-LV), discharge on

$$I_{OCL(PEAK)} = V_{OCL} \times \frac{1}{R_s} \times \frac{R_x + R_c}{R_c}$$

$OCP = 31mV * (1/9m\Omega) * ((7.5KR + 1.6KR) / 1.6KR) = 16A$

VREG5 (PIN29)
當PGOOD1 High時, 隔了7.7mS VREG5內部的LDO會被Shut Down, 改由V5SW供應5V電源. PGOOD1 Low時, 會改由內部LDO Output.

$t = C / ISS$
 $t = 0.0022\mu F / 2\mu A = 1.1mS$

SS time Setting EN1,2 pin cap

X	Standard
2200pF	1.1mS
3600pF	1.8mS
5600pF	2.8mS
8200pF	4.1mS

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Project Name: **EEV-EX14** Module Number: **PWR-04** Rev: **A0**

Size: **A3** Title: **V3.3A、V5S、V3.3S(TPS51220)** Rev: **A11**

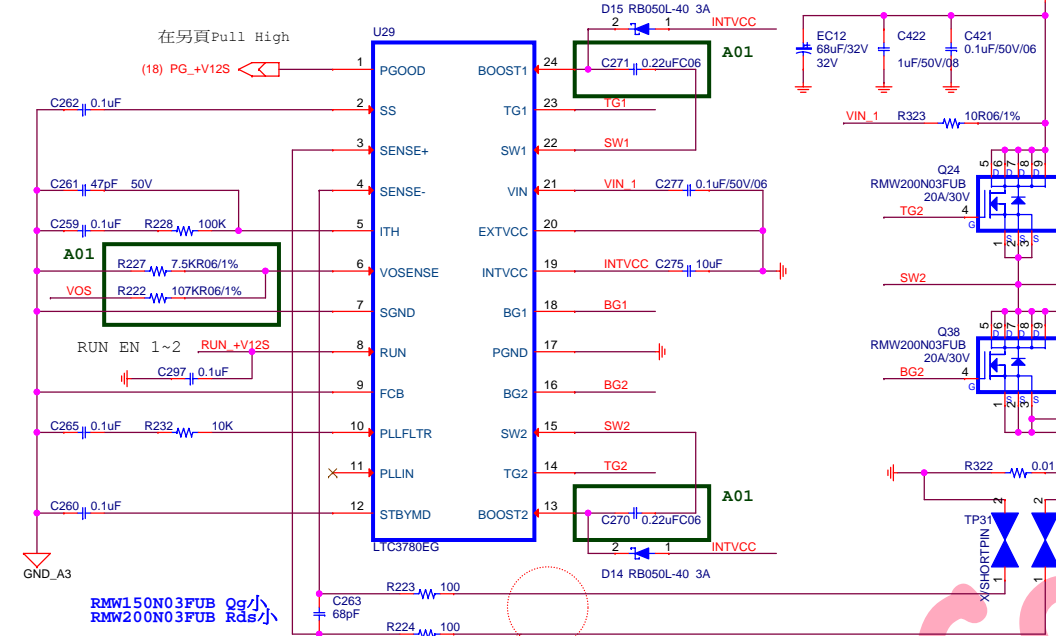
Date: **Monday, September 23, 2013** Sheet: **18** of **23**

LTC3780EG SPEC INPUT 4V~36V

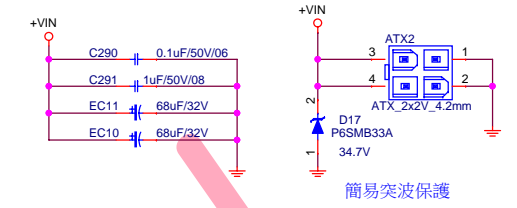
RMWxxON03FUB Vds Max 30V

+VIN SPEC INPUT 9V~28V

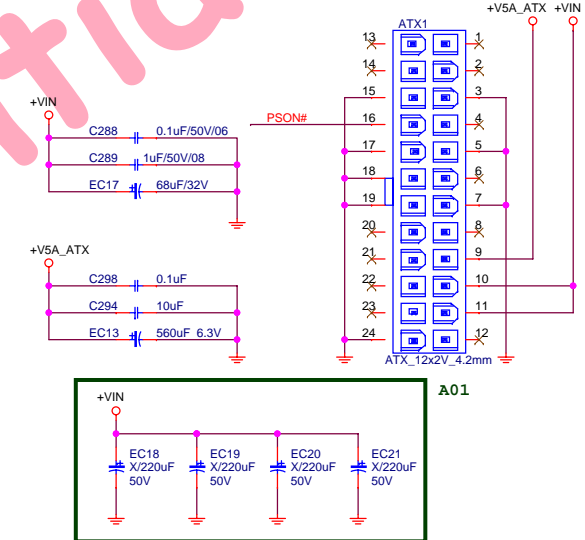
Vout=0.8x(1+107K/7.5K)=12.21V



AT POWER IN

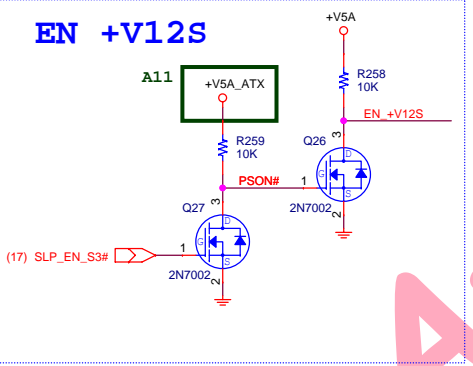


ATX Power IN

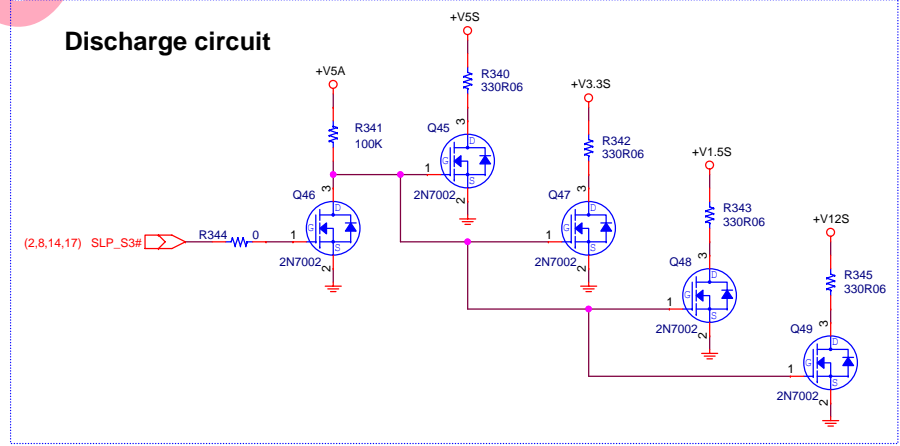


需要求走並行線10mil 線寬。
 TG1, BG1, TG2, BG2 (PIN23, 18, 16, 14) 走20mils線寬
 SW1 SW2的PLANE與其他訊號相隔至少15mils

EN +V12S



Discharge circuit



在AT POWER TYPE下：
 在未按下POWER BUTTON前，
 要先將12V送至板上，
 則需將JAT1 short PIN2、3

12V Control	Short 1、2
12V Always	Short 2、3

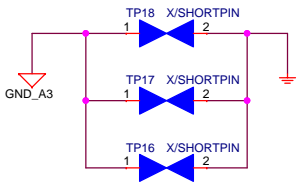
CHECK ITH及SENSE計算

VOSENSE-SET: =VOS+*Rd/(Ru+Rd)
 =12*2K/(28K+2K)
 =0.8 (為了發PGOOD)

PLLFLTR-SET: (INTVCC=6V)
 0.1.2V --> 260KHz--330KHz
 1.0.0V --> 170KHz--220KHz
 2.2.4V --> 340KHz--440KHz

FCB: Forced Continuous Control Input (less than 0.8V)
 PLLIN: External Synchronization Input to Phase Detector
 STBYMD: LDO Control Pin

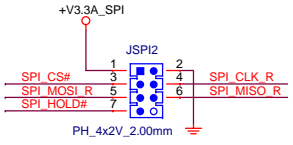
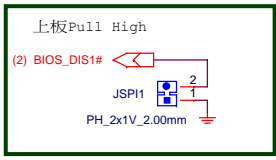
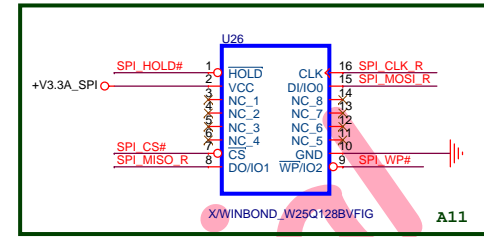
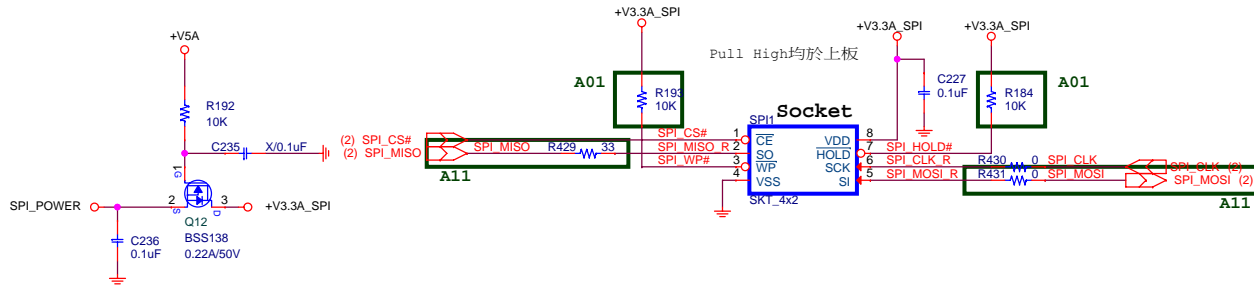
The BOOST1 pin swings from a diode voltage below INTVCC up to VOUT + INTVCC
 The BOOST2 pin swings from a diode voltage below INTVCC up to VIN + INTVCC



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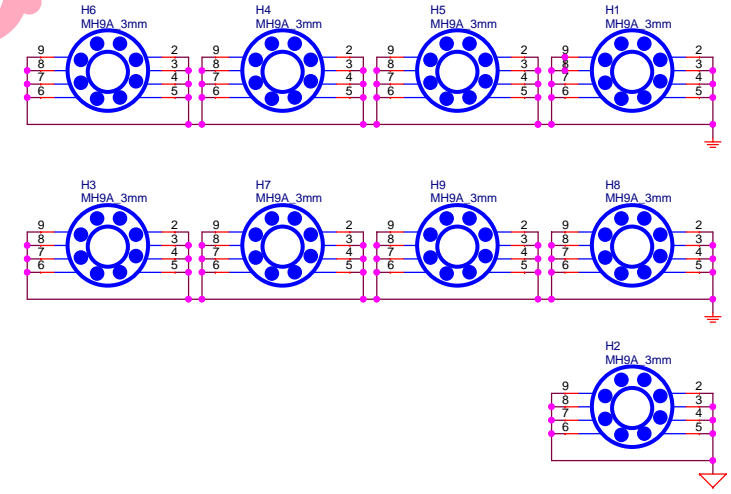
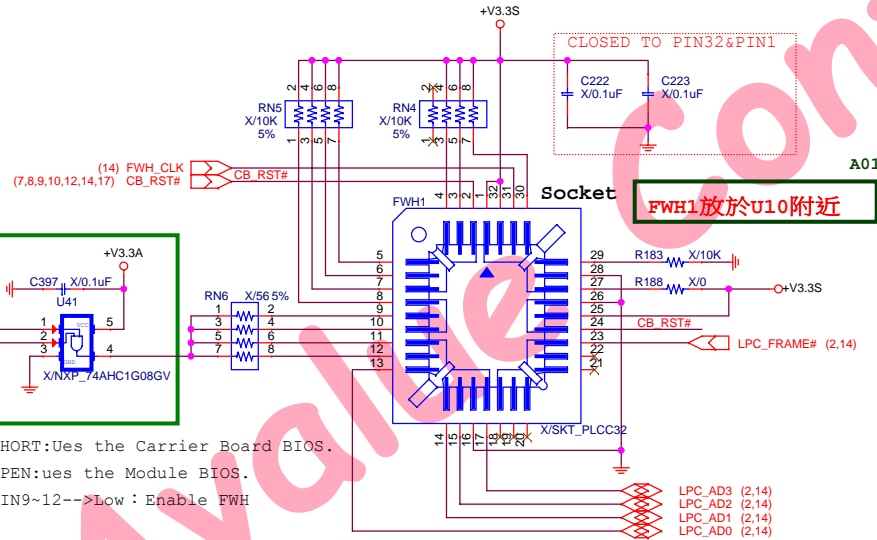
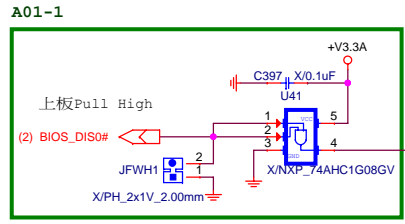
Project Name EEV-EX14		Module Number Module no. >	Rev ?
Size A3	Title ATX & AT POWER(LTC3780:12V)	Rev A11	
Date: Monday, September 23, 2013	Sheet 19	of 23	

SPI BIOS



FWH BIOS

SN74AHC1G08		
A	B	Y
H	H	H
L	X	L
X	L	L



1G08:Iout Max: 25mA SHORT: Uses the Carrier Board BIOS.
 1G125:Iout Max: 4mA OPEN: uses the Module BIOS.
 PIN9~12-->Low: Enable FWH

Table 4.13: Effect of the BIOS disable signals

BIOS_DIS1#	BIOS_DIS0#	Chipset SPI CS1# Destination	Chipset SPI CS0# Destination	Carrier SPI_CS#	SPI Descriptor	Bios Entry	Ref Line
1	1	Module	Module	High	Module	SPI0/SPI1	0
1	0	Module	Module	High	Module	Carrier FWH	1
0	1	Module	Carrier	SPI0	Carrier	SPI0/SPI1	2
0	0	Carrier	Module	SPI1	Module	SPI0/SPI1	3

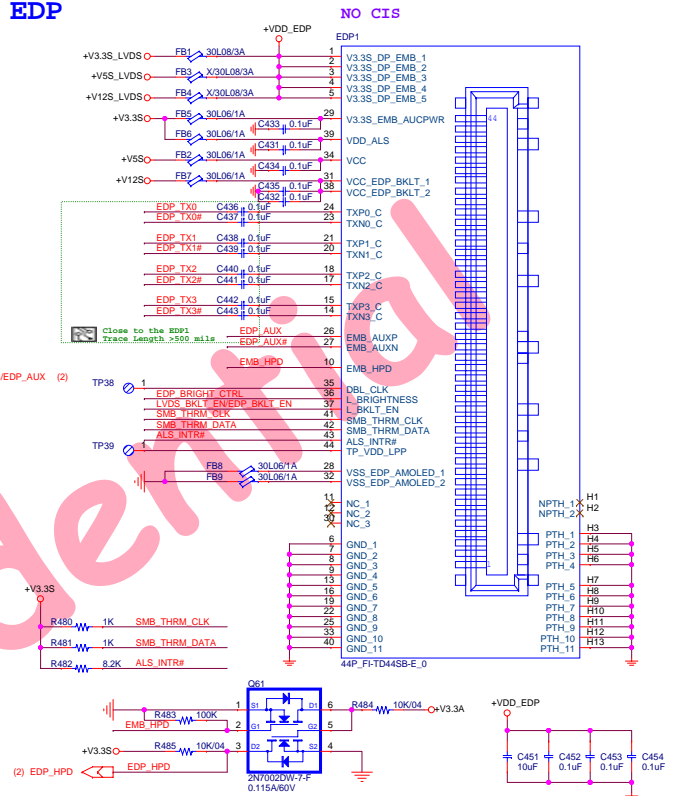
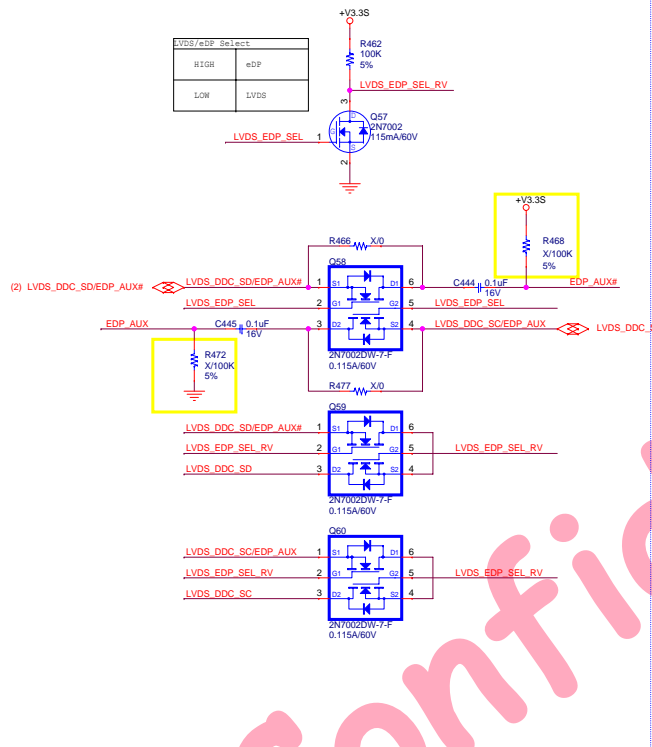
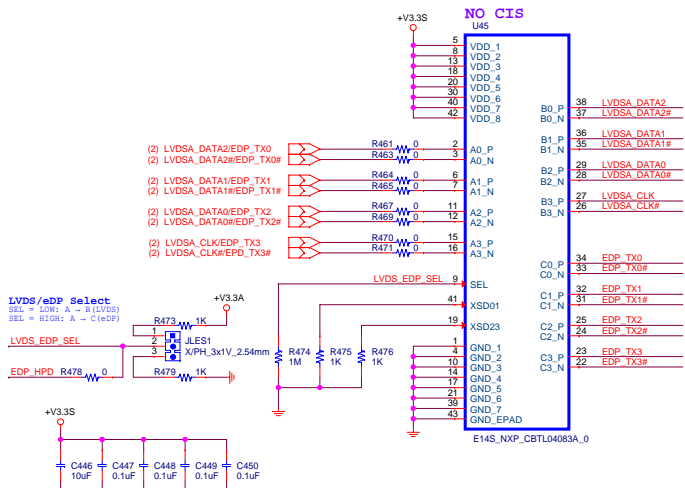
1	VPP	VCC	32
2	RST#	CLK	31
3	FGPI3	FGPI4	30
4	FGPI2	IC	29
5	FGPI1	GNDA	28
6	FGPI0	VCCA	27
7	VP#	GND	26
8	TBL#	VCC	25
9	ID3	INIT#	24
10	ID2	FWH4	23
11	ID1	RFU	22
12	ID0	RFU	21
13	FWH0	RFU	20
14	FWH1	RFU	19
15	FWH2	RFU	18
16	FWH3	RFU	17
17	GND	FWH3	17

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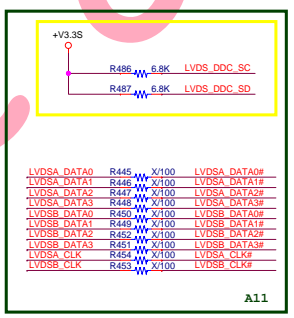
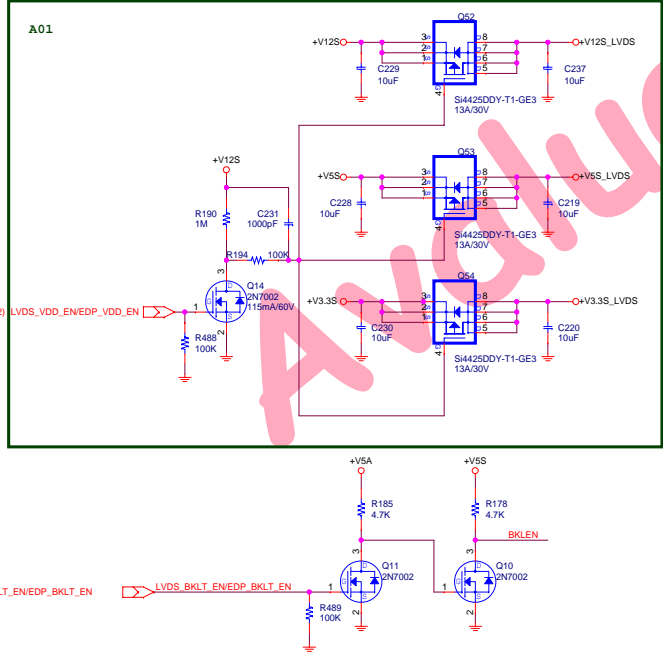
Project Name: **EEV-EX14** Module Number: **OTH-01** Rev: **A0**

Title: **BIOS(SPI - FWH)** Rev: **A11**

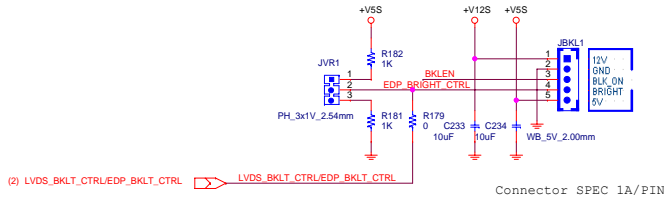
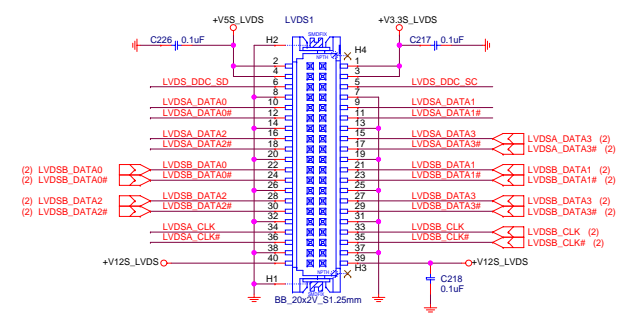
Date: **Monday, September 23, 2013** Sheet: **20** of **23**



LVDS



2	VDD3AFES	VDD3AFES	1
4	VDD3AFEB	VDD3AFEB	2
6	SFDATA	SFCLK	3
8	ON0	ON0	4
10	YAP0	YAI0	5
12	YAM0	YAIM0	6
14	ON0	ON0	7
16	YAP0	YAI0	8
18	YAM0	YAIM0	9
20	ON0	ON0	10
22	YAP0	YAI0	11
24	YAM0	YAIM0	12
26	ON0	ON0	13
28	YAP0	YAI0	14
30	YAM0	YAIM0	15
32	ON0	ON0	16
34	YAP0	YAI0	17
36	YAM0	YAIM0	18
38	CLK1M	CLK2P	19
40	ON0	ON0	20
42	VCC12	VCC12	21

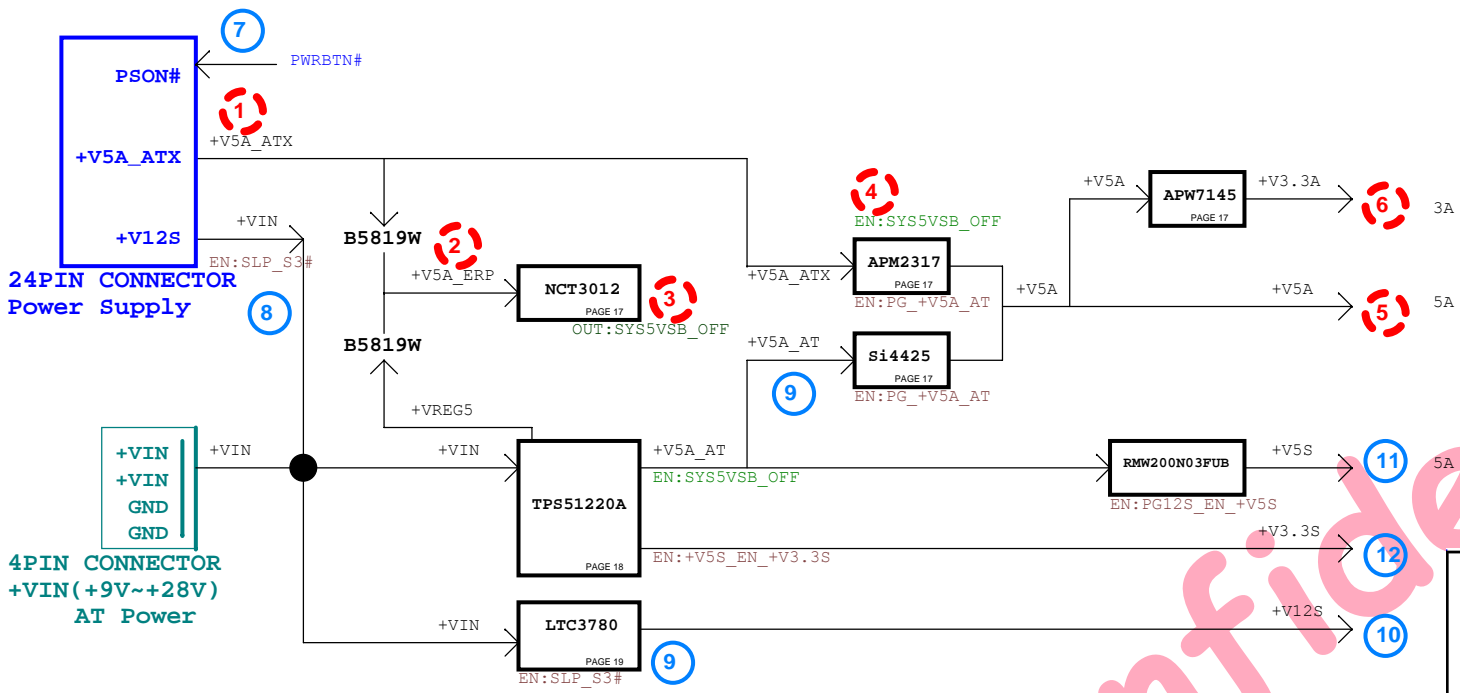


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Project Name: **EEV-EX14** Module Number: **DSP-08** Rev: **A01**

Size: **C** Title: **LVDS&EDP** Rev: **A11**

Date: **Monday, September 23, 2013** Sheet: **21** of **23**



電源選項 內容

電源配置 警告 電池計量器 進階 休眠

請選擇您要使用的省電設定。

選項

- 自動在工作列上顯示圖示(S)
- 當電腦結束待命狀態時，要求輸入密碼(P)

電源按鈕

當我關上可攜式電腦的螢幕時(W): **LID#**

待命

當我按下電腦的電源按鈕時(E): **PWRBTN#**

關機

當我按下電腦睡眠按鈕時(S): **SLEEP#**

待命

確定 取消 套用(A)

COM EXPRESS CONNECTOR

PIN(D57)	PIN(C57)	PIN(C54)	
TYPE2#	TYPE1#	TYPE0#	
X	X	X	Pin-out Type 1
NC	NC	NC	Pin-out Type 2
NC	NC	GND	Pin-out Type 3 (no IDE)
NC	GND	NC	Pin-out Type 4 (no PCI)
NC	GND	GND	Pin-out Type 5 (no IDE, no PCI)
GND	NC	NC	Pin-out Type 6 (no IDE, no PCI)

Module板對TYPE2# 接GND ~ 以示為TYPE 6 PIN DEFINE
Carrier板用此PIN來控制12V的輸出

COM EXPRESS CONNECTOR

PIN(A97)

TYPE10#

NC	Pin-out R2.0
PD	Pin-out Type 10 pull down to ground with 4.7K resistor
12V	Pin-out R1.0

Component	Voltage	Current
NCT6776F	+V3.3A	0.008A
	+V3.3S	0.025A
ALC892	+V5S	0.046A
	+V3.3S	0.012A
RTL8111E	+V3.3A	0.070A+0.100A
ICS9DB633AFLF	+V3.3S	0.250A
ASM1440 X4	+V12S	3A
	+V3.3S	0.005A*4
LAN2	+V3.3A	0.020A
EXPRESS CARD	+V3.3A	0.250A
	+V3.3S	1.000A
	+V1.5S	0.500A
MINI-PCIE Slot	+V3.3A	1.100A
	+V1.5S	0.375A
USB X6	+V5A	4.6A
FAN X3	+V12S	3A
LVDS	+V12S	3A
	+V5S	3A
	+V3.3S	2A
PCIE X16	+V12S	5.5A
	+V3.3S	3A
	+V3.3A	0.375A
PCIE X16(ADD)	+V12S	2.1A
	+V3.3S	3A
	+V3.3A	0.375A
CH7308C	+V3.3S	0.1A
	+V2.5S	0.2A
PCIE X4	+V12S	2.1A
	+V3.3S	3A
	+V3.3A	0.375A
PCIE X1	+V12S	2.1A
	+V3.3S	3A
	+V3.3A	0.375A
VGA HDMI KBMS COM2 FAN PRT FDC APW7145(1.5V/1A)	+V5S	2A

Power Rail	PCIe x1, x4 or x8 Connector	PCIe x16 Connector	ExpressCard Connector	PCIe Mini Card Connector
VCC_12V	2.1A @ 1000uF bulk	5.5A @ 2000uF bulk		
VCC_3V3	3.0A @ 1000uF bulk	3.0A @ 1000uF bulk	1.35A	1.0A
VCC_3V3_SB	375mA @ 150uF bulk	375mA @ 150uF bulk	275mA	330mA
VCC_1V5			750mA	500mA

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Project Name: **EEV-EX14** Module Number: **<Module no.>** Rev: **?**

Size: **A3** Title: **POWER DISTRIBUTION** Rev: **A11**

Date: **Monday, September 23, 2013** Sheet: **22** of **23**

MODIFY HISTORY

A0 -> A01

- 1.Page2 : Add 4 PCS 0603 0R,預留將來上下板5VSB斷開用
- 2.Page2 : Add 線路,上下板SM BUS隔離用
- 3.Page2 : Add USB3.0 Connector端0R電阻(TX RX均要)
- 4.Page3 : USB3.0之EMI Bead CK1 ~ CK8已有CIS
- 5.Page4 : Add C424(1uF),前版線路漏劃
- 6.Page4 : ALC892之BIT_CLK改放至CHIP端
- 7.Page7 : Y1(25M)改小(3.2X2.5)
- 8.Page7 : LAN1 LAN2 改料, 改使用右側雙燈 左側單燈之Connector
- 9.Page8 : SIM CARD PIN1和MIMI-PCIE1 PIN8直接接,不接至3.3A
- 10.Page8 : MINI-PCIE1的 TX對和RX對 接反修正
- 11.Page8 : U25的+V3.3S_EC和+V3.3A_EC接反修正
- 12.Page8 : APW7145的EN PIN預留0.1uF
- 13.Page9 : Add R328(0R)
- 14.Page11 : HDMI DP之EMI BEAD換廠內料(CK15~CK22)
- 15.Page11 : HDMI DP之HPD預留Pull High Pull Low電阻
- 16.Page11 : R266 100K不上件,ASM144S HPD_SINK內部已Pull Down 200K
- 17.Page12 : Add 2 PIN Header,以利插DP轉卡時,Jump不上件(斷開用)
- 18.Page13 : Add SATA3 Connector端0R電阻(TX RX均要)
- 19.Page13 : DIO Connector 電源由拉3.3A改3.3S, 並Colay Fuse限流
- 20.Page14 : OVT# Pull High由5V改接3.3V
- 21.Page14 : R42(0R)上件, SIO 內部Device Wake Function
- 22.Page14 : 更新Temperature Sensing線路
- 23.Page14 : Add U43(LPC CLOCK BUFFER)
- 24.Page16 : U21(PRINTER ESD IC)電源由V5S改接V5A
- 25.Page16 : Add EC22 EC23 EC24 : FAN Connector 12V穩壓用
- 26.Page16 : Add Q43 Q44 R333, 將上板的3.3V FANOUT(PWM) Level Shift成5V
- 27.Page17 : 預留R335(SYS_RERST# Pull High), 但不先件, 以防上板未Pull High
- 28.Page17 : 新增R334(1K-1%), ERP偵測3.3A OK後,再Delay160ms發Low Pulse用
- 29.Page17 : Add 預留R336(10K不上件) R337 R338(0R) R339(0R不上件),此狀態下板ERP仍受BIOS控制
R336(10K上件) R337 R338(0R不上件) R339(0R上件),此狀態下板ERP不受BIOS控制
- 30.Page17 : R131 R132不需上件, 因其不會影響Reset時序
- 31.Page18 : R261(0R上件),3.3V POWER GOOD要接給上板
- 32.Page18 : Q40修正其DS接反之線路
- 33.Page19 : C270 C271由用錯料的2200pF改回正確的2200nF
- 34.Page19 : R222 R227阻值調整,使輸出為12.21V(實測為12.09V, 修改前為11.89V)
- 35.Page19 : VIN預留4PCS 220uF/50V,以利高瓦特數上板使用, 如ESM-QM77
- 36.Page20 : 刪除C239(0.1uF) U26(1G125),上件R193 R184(10K),SPI_CS#由上板做控制
- 37.Page21 : LVDS POWER 改為各電源使用各自的SO8 MOS

A01-> A02

- 01.Page2 : R361 R362改連接+V5S ,
依COM SPEC --> AT時要供至上板的5VSB PIN, 可改用5V或不接
- 02.Page2 : CN1 A86、A87 保留PIN, 用0R接KB_RST#、KB_A20GATE(Super IO)
- 03.Page2 : SMB Level Shift IC Control Gate由接+V5S改+V3.3S
- 04.Page2 : CN1 PIN D97(PEG_ENABLE#)接0R至地
- 05.Page2 : CN1 PIN D54(PEG_LANE_RV#)預留接0R至地
- 06.Page7 : LAN1 & LAN2 LED線路修正
- 07.Page8 : SIM1 LAYOUT LIBRARY修正
- 08.Page8 : EXPRESS1 & EXPRESS2 舊料停產, 改料改LAYOUT
- 09.Page8 : U25 PIN1 SYSRST#(本接EXCD0_PERST#) 留0R接CB_RST#
- 10.Page8 : EXCD0_PERST# 改預留0R接至PERST#
- 11.Page15 : RS485的控制(U13)預留原來的SOUTB_IRTX, 改用RTSB#
- 12.Page19 : 新增JAT1 PIN HEADER
在AT POWER TYPE 下: 在未接下POWER BUTTON前,
要先將12V送至上板, 則需將JAT1 short
- 13.Page17 : 預設ErP不啟動(SMBUS 0R不上件) ~~ 由上板ErP運作

A02-> A1

- 01.Page03 : USB3.0的串聯0R電阻去除
- 02.Page06 : 接至Device 的PCIE TX的0.1uF已加於Module Board, 故此位置改上0R
- 03.Page17 : Power LED本接+V5A, 改+V5S
- 04.Page18 : TPS51220的EN PIN線路修改(解決ATX POWER在S5時+VIN會有5V漏電)

A1-> A11

- 01.Page02 : Modify CN1 Power in.
- 02.Page14 : Add SIO I/O address jumper select
- 03.Page17 : Modify SATA LED contorl.
- 04.Page19 : Modify PSON# contorl.
- 05.Page20 : Modify SPI connect.
- 06.Page21 : Add LVDS/eDP switch & eDP connector

		Confidential	
Project Name	EEV-EX14	Module Number	<Module no.>
Size	A3	Title	MODIFY HISTORY
Date:	Monday, September 23, 2013	Sheet	23 of 23
Rev	?	Rev	A11